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February 15, 1987 - February 14, 1988

RESEARCH ON MERCURY CADMIUM TELLURIDE

prepared for the
Defense Advanced Research Projects Agency

S.K. Ghandhi
Principal Investigator

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This report summarizes work done during the third year of a program entitled, Research on Mercury Cadmium Telluride. CdTe studies were extended to the DLTS of both n- and p- material. The wide gap materials effort was expanded with the growth of ZnSe, which is lattice matched to GaAs. Significant (100-200 times) improvement in the photoluminescence of GaAs was demonstrated by the use of a pseudomorphic ZnSe layer.

The new reactor is fully operational, and is capable of growing HgCdTe with a Cd composition control of ±0.002 across a 1 cm x 1 cm slice. In addition, significant improvement in MCT quality was obtained by the use of CdTeSe substrates. Work with CdTeZn substrates was also carried out during this year.

The work was supported by the Defense Advanced Research Projects Agency (Contract monitor: Dr. J. Murphy), and administered through the Office of Naval Research (Dr. M. Yoder). Principal authors are Professors I.B. Bhat and S.K. Ghandhi.

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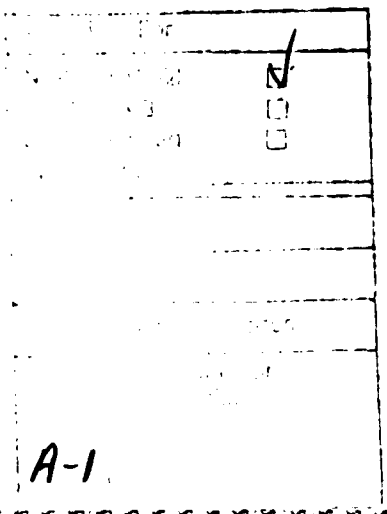

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ABSTRACT

This report summarizes work done during the Third year of a program entitled, "Research on Mercury Cadmium Telluride". Progress on the proposed tasks is outlined here, together with a review of our accomplishments. These tasks include work with our new epitaxial reactor, the growth of high quality HgCdTe on CdTeSe, CdTeZn, and CdTe substrates, and in-depth analyses of films via Double Crystal X-Ray Diffraction, Hall Effect, Photoluminescence and Deep Level Transient Spectroscopy. In addition, a start has been made on the development of characterization methods using device structures.

A new epitaxial reactor, designed during the first year, was constructed at Rensselaer. This machine is now fully operational, and is performing up to our expectations. An important goal, the growth of $Hg_{1-x}Cd_xTe$ layers with x within $\pm.002$ over a 1 cm $\times$ 1 cm area, has been met using this machine. In addition, x values within ± 0.005 over a 1 $\times$ 2 cm substrate have also been demonstrated. This work has been performed on a reactor with a stationary susceptor. A new reaction chamber, capable of rotation, has been designed and ordered. Delivery of this unit, and its use with the system, should allow layer uniformity to be achieved over larger areas.

Our work in the growth of CdTe has emphasized the development of methods for growing high quality layers by careful attention to processing conditions, and the use of double crystal x-ray and photoluminescence for characterizing these layers. Our deep level transient capacitance studies, made originally on n- CdTe, have been extended to p-type CdTe layers. Both hole and electron traps have been observed in these layers. MCT has been grown on GaAs substrates with an intervening CdTe buffer layer. This work, with x=0.27 has now been completed, and a paper written on the subject.

Both CdTeSe and CdTeZn have been explored as alternative substrates for the growth of MCT. Results with these substrates have been impressive, and a reduction

in the x-ray FWHM by a factor of 3 has been obtained.

X-ray techniques have been extensively used to determine the areal variations in lattice parameters of CdTeSe and CdTeZn substrates. We have also shown the importance of lattice match by use of this diagnostic.

This year we have placed a heavy emphasis on improved characterization methods. The Hall system has been fully automated, and a number of computer codes written to model data acquired by this system. Strain analysis with the x-ray diffraction system has also been greatly simplified by the use of computer simulation of the x-ray profile.

Both MOS and photoconductive structures are being implemented in order to measure minority carrier lifetime in MCT. Surface passivation by sulfidization and annealing methods are under active study. The sulfidization work has been successful, but annealing is still a problem area.

A number of papers have been submitted on our work. These are attached as Appendices to this report.

1. INTRODUCTION

The goal of this program is to conduct research on Mercury Cadmium Telluride and related compounds. Its emphasis is on the growth and characterization of thin films of these materials by means of Organometallic Vapor Phase Epitaxy. This report outlines tasks proposed and the accomplishments during the second year of our program.

2. WORK ACCOMPLISHED DURING THE SECOND YEAR

2.1 Reactor Development

The new reactor, which was designed during the first year, was completed during the second year, and was put into full operation this year. This system is an all welded unit capable of operation under full computer control. The reaction chamber design is a unique one, in that it eliminates all heated lines for transport of mercury into the system. Moreover, the mercury source is not in the main reactor chamber, so that it does not get contaminated by the flow of organometallic reactants over it. This combination of features has allowed reasonably good control of the Hg vapor pressure during growth, and still maintain a low level of impurities in the growing layer.

In this new design, we are using a stationary susceptor system as a cost saving feature. (The loading mechanism for this system was fabricated at a cost of $5,500, as compared to $40,000 for a system with a rotating susceptor.) This has allowed us to exceed our uniformity goals (x within ± 0.005 on a 1 cm $\times$ 1 cm slice). Moreover, x values within ± 0.005 over a 1 $\times$ 2 cm substrate have been obtained with this system.

The entire reaction chamber, including the loading and unloading mechanism, has been built as a separate module, so that it can be replaced with a more sophisticated one if future requirements necessitate this upgrade.

Successful operation of the reactor has heightened our awareness of its shortcomings, so that we have instituted a major upgrade of the system. This has been (is being)

carried out along the following lines:

1. A reaction chamber unit, with provisions for a rotating susceptor, has been designed. Construction of this unit was well beyond our capabilities, so it was farmed out to CVD Equipment, Inc. This unit has now been delivered, and should be installed soon.
2. The actual reaction chamber is also being reconfigured. This will involve some computer modelling for its optimization.
3. The gas handling on a number of the alkyl channels is being re- designed, to allow for stable operation over long periods of time.
4. The Hg chamber and the heating of this chamber are being modified to improve reproducibility.

All of these improvements should be made in the coming year, with the view towards obtaining ± 0.005 uniformity over a 2 cm $\times$ 2 cm area. The biggest problem we see here is in the logistics of making these changes with a minimum of down time.

Our research reactor, a real antique built in 1970, and perennially upgraded since then, continues to be useful in trying out new ideas with a rapid turn around time. Consequently, it is still in full use. We are, however, in the process of laying the groundwork for a totally new system, based on the atomic layer epitaxy technique. A system of this sort presents a new departure, and new possibilities for MCT growth.

A total of 100 runs were made on this reactor (System I) during the reporting period. 93 runs were made on the new machine (System V).

Mercury cadmium telluride (MCT) layers have been grown on bulk CdTe substrates, as well as on CdTeSe and CdTeZn substrates. Our results indicate that the ternary substrates have many advantages over MCT layers grown on CdTe. Work on MCT/CdTe/GaAs was confined to completing our research on the growth of $x = 0.27$ material. We certainly plan to do more work with GaAs substrates. For the present,

however, we feel that the course of research in this area should be performance driven, and have delayed the use of GaAs for this reason.

2.2 Cadmium Telluride

A considerable amount of work has been carried out in past years, on the development of high quality layers of CdTe. Specifically, these have been grown on InSb, to which it is closely lattice matched (0.07%). The resulting material is therefore of excellent crystal quality, and can be used to study the basic properties of this semiconductor. Evidence of this quality is demonstrated in the achievement of a photoluminescent peak with a FWHM of 2.1 meV at 12K, in undoped material. This value is the lowest reported for epitaxial CdTe grown by OMVPE. The PL spectrum of these layers is dominated by emissions from the radiative recombinations of the free and bound excitons, which are very well resolved. A level at 1.596 eV is associated with the recombination of free excitons. Additional levels at 1.593 eV and at 1.591 eV are also observed, and have been associated with an exciton bound to a neutral donor and to a neutral acceptor respectively. The well resolved narrow exciton band and low value of the FWHM indicate that layers are of high quality. In addition, double crystal x-ray diffraction measurements on this material has resulted in a FWHM of 20 arc seconds, with coherent epitaxy for growth at 350°C.

2.2.1 Extrinsic Doping of CdTe

Both p- and n-type extrinsic doping of these layers has been shown to be possible, using AsH_3 and $(C_2H_5)_3In$ as the acceptor and donor dopant sources respectively. With both dopants, concentration levels of 1×10^{17} cm^{-3} to 3×10^{17} cm^{-3} have been achieved. Moreover, doping is shown to be linearly related to the partial pressure of the dopant, up to 1×10^{17} cm^{-3}, indicating a low degree of compensation in these layers.

N-type layers, doped to 8×10^{15} cm^{-3}, had a 300K Hall mobility value of 900

cm^2/Vs and a 30K Hall mobility of 3500 cm^2/Vs. This is comparable to values obtained for the best bulk CdTe with the same doping level. A room temperature mobility of 80 cm^2/V-sec was measured for p-CdTe layers doped in the 3×10^{15} to 3×10^{16} cm^{-3} range. Variable temperature Hall and resistivity measurements were used to determine the ionization energy of the arsenic acceptor, which was 62±4 meV.

All our doping results were achieved by the direct addition of dopants to the reactant stream, without plasma or photo assist. This has important technological consequences, since the doping uniformity is dictated by reactor design, without the complexity of additional factors such as the beaming of optical or plasma sources. In our first experiments, a doping uniformity of ±20% was achieved over a 1.5 cm × 1.5 cm area, in a reactor with a 52 mm ID reaction chamber. We believe that this uniformity can be greatly improved, by improvements in the reactor design. These results have been outlined in Appendix A.

2.2.2 DLTS Studies of CdTe

The minority carrier lifetime is an important parameter in any optical device, so that its evaluation and measurements are important. Deep Level Transient Spectroscopy provides an important tool for this purpose. Moreover, results of the DLTS study can provide important feedback to modify the growth process.

DLTS studies of n-CdTe are relatively easy to implement, since gold provides a suitable Schottky barrier to this material. Using this approach, work with n- CdTe was carried out during the last reporting period, and is detailed in Appendix B.

DLTS studies of p-CdTe are considerably more difficult because of the lack of a suitable Schottky barrier metal. As a result, this is a research area in which very little work has been done by previous authors. In our work, n^+- p diodes were fabricated by extrinsic doping, thus allowing both electron and hole traps to be studied. A report on these studies is provided as Appendix C. We emphasize, however, that our DLTS studies of p-

CdTe are of a preliminary nature, and further work in this area should be undertaken, when time permits.

Our results show the presence of one electron trap, at 0.59 eV above the valence band. In addition, a hole trap was found at 0.58 eV below the conductance band. The emission constant of this trap was about 35 ms (at 310K), whereas complete filling of the trap required in excess of 0.7 sec, i.e., the capture rate is much larger than the emission rate. This anomalous behavior is possibly due to the presence of field enhanced emission effects, and is presently being investigated.

2.3 Growth of Zinc Selenide

Our effort on II-VI compounds has been expanded in the last year, and we have begun to explore the growth of ZnSe. This wide gap (2.7 eV) semiconductor is of technological importance because of its possible use in the blue-green spectrum. N-type doping of ZnSe is readily achievable, with Col. III dopants such as aluminum. The recently reported achievement of p-type doping has opened the door for the development of junction devices in this material.

An important characteristic of ZnSe is that it is closely lattice matched to GaAs. As a result, pseudomorphic layers can be grown on GaAs to a thickness of about 1500$\AA$. Below this thickness we can expect an interface which is relatively defect free, with an absence of dislocations. Thus, it should be possible to greatly reduce the surface recombination velocity (SRV) of the GaAs on which such layers are grown. This represents a second important use for ZnSe layers. In fact, if inversion of the GaAs could be achieved by this means, it would open the door to a true MOS technology for GaAs.

ZnSe was grown on GaAs by the reaction of dimethylzinc (DMZ) and dimethylselenide (DMSe) at a temperature of 400°C and a system pressure of 200 torr. For these runs, the partial pressure of DMZ was 0.6 torr, while that of DMSe was 1.0 torr. Layers from 800-1800$\AA$ were grown, with a growth rate of about 0.17 μm/hr. Thus, some

of these layers were thinner than the critical value for pseudomorphic growth, whereas others were thicker.

The ZnSe layers were grown on both n^+GaAs and semi-insulating GaAs substrates, on which was previously grown an epitaxial layer of GaAs by a conventional OMVPE process. Both n- and p-type GaAs layers were used, with a doping concentration of about 2.5-3 $\times$ 10^{15} cm^{-3}.

2.3.1 Photoluminescence Studies

The PL system consisted of a Ar-ion laser, a 3/4 meter spectrometer, and a photomultiplier with a liquid nitrogen cooled S-1 photocathode. This system was used to take PL data on the GaAs, and also on the GaAs with a ZnSe cap layer. The use of Ar-ion laser enabled us to study the layer close to the interface, because most of the light is absorbed by the top 0.1 μm of the GaAs. In all cases, the PL response on the ZnSe capped layers was from 100- 200 times larger than that on the bare GaAs, for cap layers of 800-1100$\AA$ in thickness. On the other hand, there was no improvement when 1800$\AA$ layers (which are thicker than the critical value), were used. Moreover, the results described here were quite reproducible. Removal of the ZnSe layer immediately eliminated the PL improvement, which was recovered by regrowth of the ZnSe cap layer.

We believe that these results can be explained by a reduction in the dangling bond concentration at the GaAs surface, due to the presence of the pseudomorphic ZnSe. Calculations of the surface recombination velocity (SRV), based on some reasonable assumptions of materials parameters, indicate a drop from 4 $\times$ 10^6 cm/sec to 1 $\times$ 10^3 cm/sec. by the use of this layer. Details of these experiments are reported in Appendix D.

Further work in this area should be directed to the growth of ZnSeS, with about 6% sulfur. This ternary compound is almost perfectly matched to GaAs, so that its growth will allow an even greater control of the dangling bond concentration at the GaAs sur-

face.

2.4 Growth of Mercury Cadmium Telluride

A small part of this year's effort was spent on completing our work on the growth of MCT on GaAs, with a high Cd content ($\simeq$27%). Here a number of additional growth runs have been made with varying CdTe buffer thicknesses, to determine the effects of this important parameter. As with previous work on x=20% layers, our results showed that a CdTe layer from 1.5-2 μm is suitable for good quality MCT growth. Details of this work have been assembled in the form of a paper which has been submitted for publication. A copy is provided as Appendix E. Our general results in this area are given in Appendix F.

2.4.2 Growth of Large Area MCT

A major part of our effort this year was centered on the growth of highly uniform MCT layers with large area (1 cm $\times$ 1 cm). In previous work, we have used CdTe substrates for this purpose. Here, the lattice mismatch between $Hg_{1-x}Cd_xTe$ with $x = 0.2$ and CdTe will generate dislocations at the interface which propagate into the epilayer. Alternative substrates, such as $Cd_{1-w}Zn_wTe$ ($w \simeq 0.04$) of $CdTe_{1-y}Se_y$ ($y \simeq 0.04$), have been proposed, which are lattice matched to $Hg_{0.8}Cd_{0.2}Te$. The addition of either Se or Zn into CdTe also increases its hardness and reduces the dislocation density of bulk grown substrates, so that these are inherently better starting materials than CdTe.

The use of Se is advantageous over Zn since it has a distribution coefficient of about 0.97, compared to 1.31 for Zn. As a result, compositional control of the substrate is maintained over larger boule lengths, so that CdTeSe is potentially a less expensive substrate material than CdTeZn. For this reason, we have chosen CdTeSe substrates for our research. Some work was, however, done with CdTeZn substrates as well, and results with both are reported here.

HgCdTe was grown by the process we have outlined in previous reports, with the exception that diisopropyltelluride was used as the tellurium source instead of diethyltelluride. This allowed growth to be carried out at an estimated substrate temperature of 370°C, with a growth rate of about 3.5μm/hr. In previous work, our growth temperature was 415°C.

Fourier transform infrared (FTIR) transmission spectroscopy has been used to study the compositional uniformity across the wafer. Initial measurements were made for us by Texas Instruments (courtesy of Dr. Carlos Castro), with subsequent data taken on our newly acquired system. The FTIR technique is nondestructive, and has a sensitivity which is comparable to or better than that of alternative methods. Measurements show that layers have edge to edge compositional uniformity (Cd fraction) of better than ± 0.005 (standard deviation = 0.0024) over the whole area, and better than ± 0.002 (standard deviation = 0.0014) over a 1 cm $\times$ 1 cm area. The thickness uniformity of the layer is also excellent, better than ± 0.7 μm for 12-μm thick layers. Many layers have been grown with a composition of $x \simeq 0.2$, and the uniformity was found to be reproducible from run to run.

We believe that this is the first time such compositional uniformity has been demonstrated over this large area, using conventional alloy growth techniques by OMVPE. Layers of comparable uniformity have been grown using an interdiffused multilayer process (IMP), where alternate layers of CdTe and HgTe are grown under optimized growth conditions for each binary compound, and homogenized at the growth temperature with an annealing step. The crystallinity of interdiffused HgCdTe has been shown to be poorer than that of alloy grown HgCdTe, as determined by double crystal x-ray diffraction. This has been attributed to crystalline defects generated due to the lattice mismatch between HgTe and CdTe, and to incomplete interdiffusion. Thus, the conventional alloy growth technique is potentially more suitable for devices, if compositional

uniformity is achieved as demonstrated here.

Double crystal diffraction measurements, made on these layers, confirm the advantage of using CdTeSe substrates over CdTe. Typically, FWHM values of 47±2 arc sec. were obtained on CdTeSe, as compared to 151±15 arc secs. when CdTe substrates were used. This improvement comes about because of two reasons. First, the CdTeSe substrates had FWHM values of ≈14 arc secs., whereas CdTe substrates had values of about 32 arc secs. Thus, in addition to CdTeSe being a better lattice match to HgCdTe, its crystal quality is superior to that of CdTe. We believe, however, that the significant improvement in the quality of HgCdTe layers grown on CdTeSe substrate is primarily due to its better lattice match to the substrate. This is shown in the next section.

2.4.3 X-ray Diffraction Studies of MCT

These studies were carried out in order to determine the effect of variations in the compositional uniformity of the starting substrates. For this work, we used CdTe, CdTeSe and CdTeZn substrates. In all cases, very thin (3 μm) layers of MCT were grown, so that the x-ray peaks associated with the MCT and the substrate could both be observed. The separation between the two x-ray peaks was taken as a measure of the lattice parameter differences between the layer and substrate.

As previously noted, our compositional change over a 1 cm × 1 cm slice is within ±0.002. This corresponds to an x-ray separation of ±8 arc- sec. For these experiments, small slices, 0.5 cm × 0.5 cm were used, so that we can assign somewhat less than ±8 arc sec. shifts to our own system tolerance.

With all samples, x-ray measurements were taken at three points across the slice. The data for these measurements is shown in Table I. Here we note the following:

1. Layers grown on CdTe had the largest x-ray separation, as expected. However, this separation was the same at the three points which were measured. This indicates that the composition uniformity of the grown layer is excellent.

TABLE I

SUBSTRATE AND LOCATION	FWHM OF MCT (arc sec)	FWHM OF SUBSTRATE arc sec	$\Delta\theta$ arc sec
CdTe: A	187	47	+320
B	175	45	+320
C	210	100	+320
CdTeSe: A	63	– – –	$\simeq 0$
B	59	– – –	$\simeq 0$
C	65	– – –	$\simeq 0$
CdTeZn: A	126	53	−198
B	151	63	−155
C	127	37	−170

TABLE II

x Cd	t microns	FWHM of MCT (arc sec)
.23	3.2	110
.267	3.1	76
.27	3.1	55
.31	3.0	110

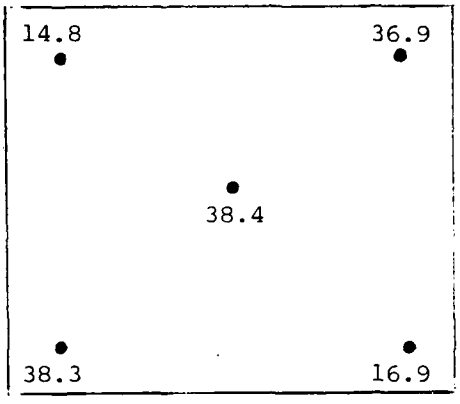

Figure 1(a) X-ray FWHM of CdTeSe substrate (in arc-sec).

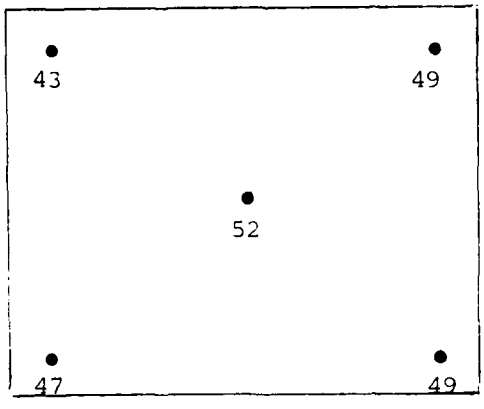

Figure 1(b) X-ray FWHM of MCT (x=0.27) layer grown on CdTeSe substrate, shown in Fig. 1(a) (in arc-sec).

2. Layers grown on CdTeSe were exactly matched at all points. A lucky break, but again indicative of uniformity of the MCT layer.
3. The layer grown on CdTeZn had x-ray separations ranging from -155 to -198 arc-sec. indicative of changes in the composition of the substrate. Moreover, the lattice parameter of this substrate was smaller than that of HgTe, as evidenced by the negative values measured on our x-ray system.

As expected, this data also shows that the FWHM of the lattice matched MCT is the lowest, whereas that of the grossly mismatched system (MCT-CdTe) was the largest. The CdTeZn layer gave intermediate results, as can be expected.

We have also studied the effect of lattice mismatch on the FWHM of MCT layers. This was done by growing a series of MCT layers, of different composition, on pieces from the same CdTeSe substrate, which we assume to have a uniform Se composition. Again, thin layers ($\simeq$3 μm thick) were grown to emphasize the effect of the mismatch. Table II shows the FWHM as a function of the MCT composition. Here, a perfect match (x=0.26-0.27) resulted in a FWHM of 55-76 arc sec., whereas a FWHM of 110 arc-sec. was obtained for x values of 0.23 and 0.31. This clearly establishes the advantage of using a lattice matched substrate for the growth of MCT.

A study was also made on the effect of CdTeSe quality on the FWHM of MCT layers, to give us an idea of how much the non-uniformity in the quality of the substyrates affects the MCT layer. Figure 1(a) shows the FWHM map of the CdTeSe substrate, before any layer was grown. An x-ray FWHM map, after the growth of $\sim$7 μm thick MCT (x = 0.23) is shown in Fig. 1(b). It is seen from the data that small variations in the x-ray FWHM of the substrate do not affect the MCT layer quality, as long as this FWHM value is below a certain value ($\sim$38 arc seconds). Other factors such as lattice matching or the actual growth process will determine the MCT layer quality.

2.4.4 Intrinsic Doped MCT

Both n- and p-type layers can be grown, depending on our reactor process. Uncapped layers, annealed in situ at 300°C in a Hg overpressure, were n-type. These layers had a background concentration below 1×10^{15} cm^{-3}, with a 20K mobility of 6×10^5 cm^2/Vs., indicating a low level of background contamination due to the starting chemicals. We feel quite confident that this background concentration will drop by a decade or more, as purification techniques for DIPT are advanced by its manufacturers.

p-type layers were grown when a 0.5μm thick cap of CdTe was grown as a protective coating on the MCT. This serves to "seal in" the Hg vacancies, which are shallow acceptors. These samples showed classical p-type behavior. The hole carrier concentrations for these layers was around 5×10^{16} cm^{-3}, with 77K hole mobilities in the 400-650 cm^2/Vs range. The actual hole concentration was a function of the Hg-overpressure, which is not under as tight control as we would like it to be. Some reactor changes are being considered to rectify this problem.

The results of our work in this area are outlined in Appendices G and H. A review paper of the area is given in Appendix I.

2.5 Characterization

Characterization is an important component of any program of materials research, since it provides the necessary information which can be used to modify the growth process. As our growth techniques become more refined, we see a greater need for an improvement in this area, and have consequently increased our effor' on this phase of the program. Currently, a number of characterization tools have been acquired/developed for our work. Some of these are now detailed.

2.5.1 Fourier Transform IR Spectroscopy

Fourier Transform IR Spectroscopy continues to be a valuable tool for the measurement of layer thickness and composition. Our instrument, a Mattson Cygnus 100, is

computer controlled so that measurements can be made at as many as 100 points over a 1 cm $\times$ 1 cm sample. Both composition and layer thickness can be determined with this instrument.

Layer thickness of MCT films grown on CdTe/GaAs are complicated by the fact that three different refractive indices must be considered. A computer program has been written to analyze the complex fringe structure which is obtained under these conditions. In addition, other codes are being developed for the estimation of composition grading in the MCT, by means of this tool.

2.5.2 Double Crystal X-ray Diffraction

Double crystal x-ray diffraction, using (004) reflections, is routinely used to measure layer quality. Recently, we have developed methods for taking low angle measurements, using (115) reflections. This is useful for very thin layers, and also for corroborating strain measurements of MCT films. Computer codes have been written to simulate rocking curves in the presence of strain. When completely debugged, these will allow a detailed analysis to be made of the x-ray data.

2.5.3 Hall Effect

Hall effect measurements give a quick idea of both crystal quality and background concentration. For n-type samples, measurements at a few points from 10-300K can provide enough data for sample evaluation. p-type samples, on the other hand, require a detailed plot over this temperature range. Moreover, anomalous results often arise, especially in lightly doped, low x, layers which are subject to surface inversion.

During the last year we have completely automated our Hall effect system so that it is now under full computer control. This has greatly improved our data acquisition capability. In addition, a number of computer programs have been written for p-MCT, since the results of the Hall measurements can best be evaluated by fitting of the data to a theoretical model.

2.5.4 Annealing Experiments

Since MCT is a defect semiconductor, its electrical properties are a function of both process conditions as well as of impurities which are either accidentally incorporated as contaminants, or purposely introduced as extrinsic dopants. Thus, it becomes important to eliminate intrinsic defects if we are to study the effects of extrinsic impurities.

MCT growth is usually carried out in a Hg-deficient environment, so that the growing material is p-type. During cool-down, however, it is subjected to a Hg-rich ambient, so that it is partially converted to n-type. These complications can best be avoided if defect control is carried out by annealing samples after they are grown.

A number of experiments have been carried out to develop a suitable method for annealing thin layers of MCT. An annealing system has been set up, using sealed quartz ampoules in which a small amount of Hg is incorporated to provide a suitable overpressure. After sealing, the tubes are heated for 24-48 hours, and then cooled in a controlled manner.

Our annealing experiments have met with only partial success at the present time. Best results have been obtained when cooling is carried out at an extremely slow rate. This is done by shutting off the power to the furnace, (which has a high thermal mass), and allowing it to cool over a period of several hours. Even so, a complete conversion to n-type was not achieved. Further annealing experiments will be undertaken in order to improve on this process.

2.5.5 Lifetime Measurements

This is the single area in which we have the greatest need for materials characterization, and simultaneously the greatest weakness. Two approaches are under development at the present time. The first of these involves the fabrication of photoconductor (PCD) devices, from which the lifetime can be extracted by taking steady state photo-response measurements. Although simple in principle, this approach is fraught with experimental

difficulties, so that only a few devices are useful.

A mask set has been made to allow the fabrication of 16 devices simultaneously in view of the low yield of this process. Both photolithography and sample delineation techniques have been developed for this purpose. Mounting of the chip to a cold finger in a dewar, and connection of the devices to the outside world, is the next step. Techniques for doing this have also been developed. Finally, an IR source, and the associated equipment (choppers, lock-in amplifiers, and monochromators) have been assembled in order to take these measurements. Using this approach, we have begun to make spectral response measurements of our material, from which the minority carrier lifetime can be obtained.

A second approach we are also pursuing is the measurement of MOS capacitance transients. This approach is inherently simpler, since it is purely electrical in character; moreover, it involves less device processing steps than the PCD approach. In both cases, however, it is necessary to develop a method for passivating the MCT surface, otherwise the lifetime will be dominated by this parameter.

We have explored a number of surface coatings for this purpose. Of these, our greatest success has been the use of a sulfidization methods for passivating the MCT surface. This method is a modification of the one proposed by Nemirovsky et. al. We have found it especially suitable for p-type layers and are using it for lightly doped MCT.

The sulfidized layer, which is essentially CdS, is not suitable by itself as the insulator of an MOS structure. Consequently, it is covered with a ZnS cap prior to the evaporation of dots for making the MOS structure.

3. PAPERS AND PRESENTATIONS

We believe that the dissemination of research findings to the technical community

is an important part of a university program such as ours. As a result, a number of papers, based on our work during this year, have been submitted to the professional journals. These are listed, together with their current status. In addition, presentations on this work have been made to DARPA and also at professional society meetings.

Publications:

1. N.R. Taskar, V. Natarajan, I.B. Bhat and S.K. Ghandhi, "Extrinsic Doped n- and p-type CdTe Layers Grown by Organometallic Vapor Phase Epitaxy", J. Crys. Growth, 86, 228 (1988).
2. S.K. Ghandhi, S. Tyagi and R. Venkatasubramanian, "Photoluminescence of GaAs in ZnSe/GaAs Heterojunctions Grown by Organometallic Epitaxy", Appl. Phys. Lett., (submitted).
3. V. Natarajan, N. Taskar, I. Bhat, and S.K. Ghandhi, "Growth and Properties of HgCdTe on GaAs, with $x \simeq 0.27$", J. Electron. Matls, (submitted).
4. I.B. Bhat, N.R. Taskar, K. Patel, J.E. Ayers and S.K. Ghandhi, "Characteristics of OMVPE-grown CdTe and HgCdTe on GaAs", Proc. of the SPIE, 796, 194 (1987).
5. S.K. Ghandhi, I.B. Bhat, H. Fardi, "Organometallic Epitaxy of HgCdTe on CdTeSe Substrates with High Compositional Uniformity, Appl. Phys. Lett., 52, 392 (1988).
6. I.B. Bhat, H. Fardi, S.K. Ghandhi and C.J. Johnson, "Highly Uniform, Large Area HgCdTe Layers on CdTe and CdTeSe Substrates", J. Vac. Sci. Tech., (accepted).

Presentations:

1. S.K. Ghandhi, "The Organometallic Epitaxy of HgCdTe for Infrared Detector Applications", Materials Research Society Meeting, Boston, MA, Nov. 30-Dec. 5, 1987.
2. V. Natarajan, N. Taskar, I. Bhat and S.K. Ghandhi, "Growth and Properties of HgCdTe on GaAs", 3rd International OMVPE Workshop, Brewster, MA, Sept. 21-23, 1987.

3. S.K. Ghandhi, "The Epitaxy of CdTe and HgCdTe", 3rd International OMVPE Workshop, Brewster, MA, Sept. 21-23, 1987.
4. I.B. Bhat, H. Fardi and S.K. Ghandhi, "Highly Uniform, Large Area HgCdTe Layers on CdTeSe Substrates", 1987 U.S. Workshop on the Physics and Chemistry of Mercury Cadmium Telluride, New Orleans, LA, Oct. 6-8, 1987.
5. W.I. Lee, N.R. Taskar, J.M. Borrego and S.K. Ghandhi, "DLTS Studies of n and p CdTe", 1987 PVR&D Meeting, Denver, CO, Nov. 16-18, 1987.
6. N.R. Taskar, V. Natarajan, I.B. Bhat, J.M. Borrego and S.K. Ghandhi, "Extrinsic Doped n- and p-Type CdTe Layers Grown by Organometallic Vapor Phase Epitaxy", American Assn. of Crystal Growth Meeting, ACCG-7, Monterey, CA, July 12-17, 1987.
7. H.G. Bhimnathwala, N.R. Taskar, W.I. Lee, I.B. Bhat, S.K. Ghandhi and J.M. Borrego, "Photovoltaic Properties of CdTe Layers Grown by OMVPE", 19th IEEE Photovoltaic Specialists Conference, New Orleans, May 4-6, 1987.

4. PLANS FOR THE NEXT YEAR

1. Large area HgCdTe. This will be the main focus of our growth effort. Both CdTe, as well as lattice matched substrates such as CdTeZn and CdTeSe, will be considered. A new reaction chamber, incorporating a rotating susceptor, will be installed in placed of our existing unit.

   We plan to explore a new tellurium source, methylallyltelluride, during this phase of the program. This should allow further reduction of the growth temperature. Other chemicals will also be considered, if time permits.

   The growth of CdTeSe will also be initiated. We believe that this will be a superior buffer layer to CdTe, which is presently being used for our MCT on GaAs work.
2. Doping of HgCdTe. Here both p- and n-doping will be considered, with the focus of

our effort on p-doping. Arsine gas will be used for this purpose. Further work will be done on improving our annealing system, since an anneal step is required for the purpose of evaluating the doped material.

3. Materials Characterization. Research in this area will emphasize the measurement of minority carrier lifetime. Work will proceed along the lines outlined in this report.

5. ANTICIPATED PROBLEMS

Our work is progressing satisfactorily and we do not anticipate any major problems in the growth area. A potential problem, however, is that of managing the switch-over from a stationary susceptor reaction chamber of proven quality, to a new, improved chamber that is yet untested. The down- time associated with this step is of major concern to us. This is a serious problem, since the demand on our material, both by our group and by outsiders to whom we have made it available for evaluation, is continually increasing.

The diagnostics of minority carrier lifetime is a continuing problem. New approaches are under consideration, but are being delayed since their implementation would place an excess burden on our modest budget.

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EXTRINSIC DOPED n- AND p-TYPE CdTe LAYERS GROWN BY ORGANOMETALLIC VAPOR PHASE EPITAXY

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In this paper we report on the extrinsic n- and p-doping of CdTe layers, grown by organometallic vapor phase epitaxy. Triethylindium and arsine gas were used as n- and p-type dopants respectively, with doping levels of around $10^{17}\,cm^{-3}$ in both cases. Layers were grown on both semi-insulating CdTe and GaAs substrates. Layers grown on semi-insulating GaAs had an intervening 1–2 μm undoped CdTe layer to relieve the strain caused by the large (14.6%) lattice mismatch of the CdTe–GaAs combination. Van der Pauw measurements were made to evaluate the quality of these layers, and mobility values as high as 3600 $cm^2/V\cdot s$ obtained at 40 K for lightly doped n-type samples. Grown junctions, made using extrinsic doped layers, have resulted in diodes with excellent electrical characteristics.

1. Introduction

Considerable interest has been shown in CdTe as a potential candidate for efficient solar cells and other optoelectronic devices [1,2]. This material can be produced in both n- and p-type, and p–n junction devices can be realized. Recent interest has been emphasized in the epitaxial growth of this material. Hence, it is necessary to have the ability to dope the layers during growth and to control their doping profile. This is especially true for structures such as back-surface field enhanced solar cells, where a doping gradient is used to increase the open circuit voltage. Extrinsic doping is the best technique to achieve this goal. Recently, indium and antimony doping of CdTe has been reported in a molecular beam epitaxial system [3,4]. However, it was necessary to use a laser-enhancement to effect doping in these films.

In this paper we describe the In and As doping of CdTe in an organometallic vapor phase epitaxial (OMVPE) system, and the characteristics of the p–n junction devices fabricated with these dopants. Doping levels up to $1\times10^{17}\,cm^{-3}$ have been reproducibly obtained in n-type material. We have already reported on the p doping of CdTe up to a level of $2\times10^{17}\,cm^{-3}$ in this system [5]. Here we will report on some recent results on the growth of the p-type layer.

2. Experimental

CdTe growth was carried out in an atmospheric pressure reactor using diethyltelluride (DETe) and dimethylcadmium (DMCd) as the Te and Cd sources. A $25\times20\times60$ mm RF heated graphite susceptor, with a smoothly sloping front surface, was used in a 52 mm diameter horizontal reactor tube. Partial pressures for DMCd and DETe ranged from 2×10^{-4} to 5×10^{-5} atm in this study. Triethylindium (TEIn) and arsine were used as the n-type and p-type dopants, respectively. Substrates were (100)2° → (100) oriented semi-insulating GaAs. Undoped CdTe substrates of the same orientation were also used for some of the experiments. The GaAs substrates were degreased using standard solvents and etched in a solution of $H_2O:H_2O_2:H_2SO_4$ (1 : 1 : 5 by volume) for 5 min, prior to loading into the reactor. CdTe substrates were etched in a 1% bromine–methanol solution.

A buffer layer of undoped CdTe was grown on GaAs at 350 °C before the growth of the doped layer. This buffer layer was verified to be of high resistivity, so that the effects of this layer on the electrical properties of the doped layer could be neglected. Hall mobility and resistivity measurements were made over the temperature ranges from 15K to 300 K with a magnetic field strength of 4.5 kG, using the Van der Pauw technique. A

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cloverleaf pattern was delineated in the epitaxial layer for this purpose. Ohmic contacts to n-type layers were made by alloying In pellets at 180°C for 5 min. in a reducing ambient. Ohmic contacts to p-type layers were made by electroless deposition of nickel, followed by indium solder [6]. Some difficulty was observed in making contacts which were ohmic down to 100 K, in the case of lightly doped p-CdTe.

3. Results and discussions

3.1. n-Type layers

Semi-insulating GaAs substrates were used for all indium doping experiments. A 1 μm thick undoped CdTe layer was first grown at 350°C followed by a 6 μm thick doped layer at 420°C. From our earlier work, we have found that a 1 μm thick buffer layer relieves most of the strain caused by the lattice mismatch between the CdTe and GaAs [6,7]. In addition, the presence of this undoped layer prevents accidental doping by gallium from the substrate. Secondary ion mass spectrometry studies, carried out on CdTe grown on GaAs at doping temperatures, have shown negligible out-diffusion of Ga from the substrate, beyond 0.5 μm. Moreover, the breakdown voltage between 0.3 mm diameter gold Schottky metal contacts deposited 0.2 cm apart on undoped CdTe layers grown on GaAs, was found to be in excess of 400 V, which indicates its semi-insulating nature. Hence, the doped layer alone has been taken as the active layer in calculating the mobility and carrier concentration.

Fig. 1 shows the free electron concentration in In doped layers, measured at 300 K, as a function of TEIn partial pressure. The partial pressure of TEIn was varied from 1×10^{-8} to 3×10^{-5} atm, while the partial pressure of DETe and DMCd were held at 5×10^{-4} and 2×10^{-4} atm, respectively. Here, the carrier concentration increases linearly with the TEIn flow rate at low doping levels and saturates at an electron concentration of about 1×10^{17} cm^{-3}. The saturation value is a function of the growth temperature and the partial pressure ratio of DETe to DMCd, so that higher doping levels can be obtained by optimizing the reactant partial pressures and the growth temperature. We have seen that, as the DETe pressure is increased relative to the DMCd partial pressure, the doping level also increases. Since In occupies Cd sites, higher Te pressure will increase its incorporation into these sites. Residual doping from DETe can be ruled out in this case because no doping was found when TEIn was absent. Growth

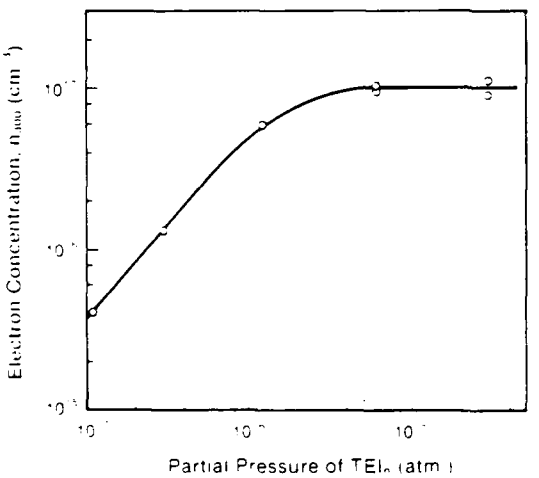

Fig. 1. Room temperature carrier concentration as a function of partial pressure of TEIn.

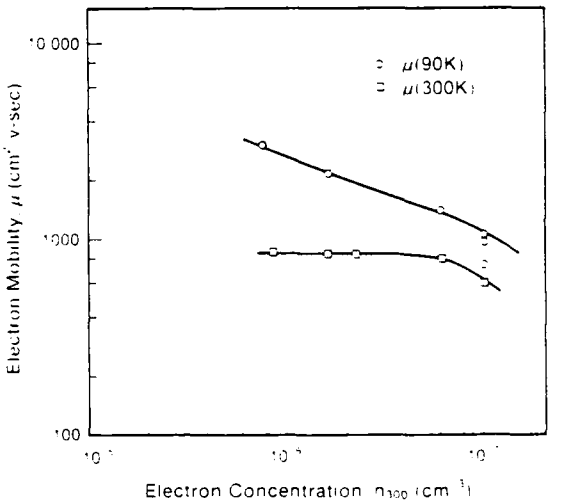

Fig. 2. 90 K and 300 K electron mobility of n-type CdTe layers as a function of doping level.

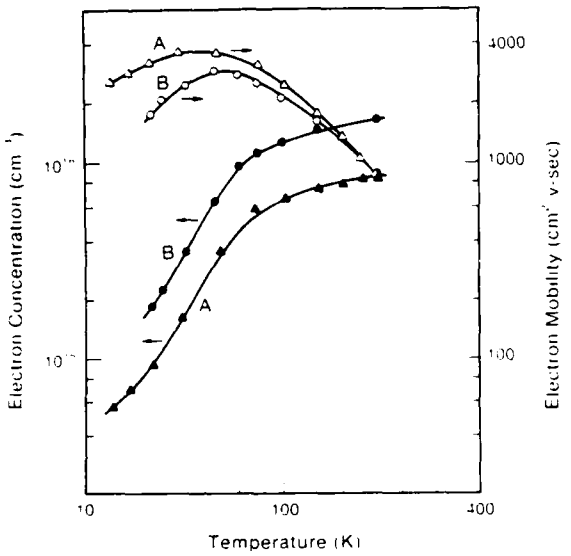

Fig. 3. Electron mobility and carrier concentration of two n-type layers, A and B, as a function of sample temperature.

at a lower temperature gave lower carrier concentrations, probably because TEIn is relatively stable below 420 °C [8].

The 90 and 300 K electron mobilities are plotted as a function of the carrier concentration in fig. 2. The 90 K mobility monotonically decreases as the carrier concentration is increased, since ionized impurity scattering dominates in this region [9]. The data points for a doping level of 1×10^{17} cm^{-3} show decreasing mobility for layers grown with higher TEIn flows. This indicates that layers grown with large flows of TEIn are compensated, probably due to an acceptor level related to In. The room temperature mobility value was found to be independent of the carrier concentration, for doping levels below 1×10^{17} cm^{-3}. These values are comparable to those obtained for bulk CdTe [9].

Van der Pauw measurements were made over a temperature range from 15 to 300 K. Fig. 3 shows the Hall mobility and the carrier concentration as a function of temperature, for two representative samples. The room temperature mobility of both these samples was about 900 $cm^2/V \cdot s$. The maximum in the Hall mobility was observed at about 30 K for the more lightly doped sample, with a value of about 3600 $cm^2/V \cdot s$. Freeze-out of the carriers was observed below 100 K. The electrical characteristics of these samples are similar to that of the best bulk CdTe with similar doping levels [9,10].

3.2. p-type layers

Arsine in hydrogen was used to dope the layers p-type. Both undoped CdTe substrates and semi-insulating GaAs substrates were used, and the growth was carried out at 350 °C. The use of undoped CdTe substrates did not give consistent results for lightly doped layers. This is because the substrate itself is slightly p-type; thus shunting effects result in data which are difficult to interpret. For these low doped p-type layers, a buffer layer of undoped CdTe was grown on semi-insulating GaAs, in order to relieve the stress caused by lattice mismatch. All active, doped layers of CdTe described here were 4.5 μm thick.

Fig. 4 shows the room temperature carrier concentrations and the mobility as a function of the arsine flow. The doping level increases linearly with the arsine flow rate, and saturates at a value of 8×10^{16} cm^{-3}. By increasing the DMCd to DETe partial pressure ratio, we were able to obtain doping levels as high as 2×10^{17} cm^{-3}. From the variable temperature Hall and resistivity measurements, and from the photoluminescence mea-

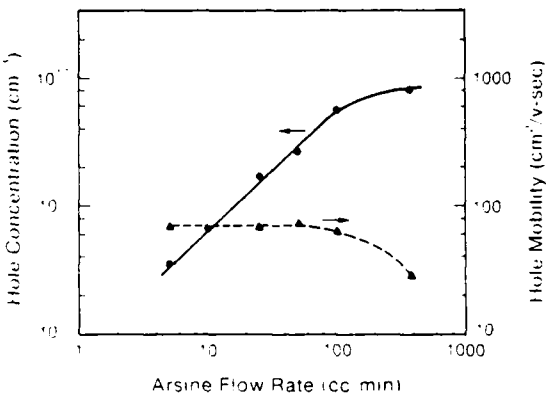

Fig. 4. Room temperature hole concentration and hole mobility as a function of arsine partial pressure. Note that 60 SCCM arsine flow corresponds to 1×10^{-4} atm of pure arsine.

surements, the ionization energy of the arsenic acceptor was estimated to be about 62 ± 4 meV [11].

3.3. p–n Junction devices

Fig. 5 shows the characteristics of a p–n diode grown on this system. The diode structure consisted of a 3 μm thick n-type layer followed by a 3 μm thick p-type layer, grown on an InSb substrate. Ohmic contact to the p-type layer was made by electroless deposition of gold. The diode size was 0.7 mm × 0.7 mm.

The I–V characteristic of a diode of this type is shown in fig. 5, and indicates a breakdown voltage of 10 V. Room temperature capacitance–voltage (C–V) measurements on this diode show an effective doping of 1×10^{15} cm^{-3} in the n-layer and a built-in voltage of 1.2 V. The p-doping concentration on a similarly doped sample was measured to be 1×10^{17} cm^{-3}. These values for the doping give a theoretical value of 1.2 V for the built-in voltage. Forward and reverse $\ln(I)$–V measurements made on this diode show an ideality factor of 1.04 at a forward bias above 0.4 V, and a saturation current density of 1.3×10^{-12} A/cm^2. The reverse leakage current was 10 pA. These values indicate that diodes of excellent quality can be made by extrinsic doping of CdTe layers.

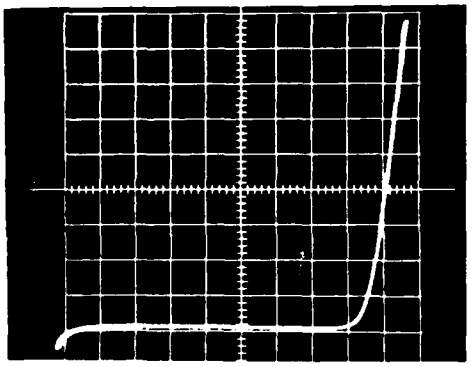

Fig. 5. I–V characteristic of a p–n junction diode. Current scale 0.1 mA/div. Voltage scale: 0.2 V/div forward; 2.0 V/div reverse.

4. Conclusion

Both n- and p-type doped CdTe layers have been grown using the extrinsic dopants In and As respectively. TEIn was used as the In source and good control of the doping was obtained up to a level of 1×10^{17} cm^{-3}, at a growth temperature of 420 °C. Beyond this point, the doping level was found to saturate, probably due to an In related compensating acceptor. The doping efficiency was lower at lower temperatures, probably because of the stability of the TEIn reactant source. Hall mobility and carrier concentration was measured for these samples as a function of temperature. Mobility values as high as 3600 cm^2/V·s at 30 K was obtained for samples with a room temperature carrier concentration of 8.2×10^{15} cm^{-3}.

p-type layers were grown using arsine as the doping gas. Doping levels as high as 2×10^{17} cm^{-3} were obtained at 350 °C, and the arsenic acceptor level was estimated to be 62 ± 4 meV above the valence band. p–n Junction devices were fabricated by using the above doping techniques. The results show the suitability of OMVPE for fabricating high quality devices in CdTe.

Acknowledgements

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DLTS STUDIES OF N-TYPE CdTe GROWN BY ORGANOMETALLIC VAPOR PHASE EPITAXY

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ABSTRACT

Deep levels in n-type CdTe layers, grown by OMVPE on InSb substrates, have been investigated using DLTS technique. A total of five levels were detected and four of them appeared on all the samples (E2 = 0.36eV, E3 = 0.65eV, E4 = 0.74eV, E5 = 1.15eV). The growth condition dependence of the deep level concentrations provides important information about the origins of these levels. The very deep level E5, which has never been reported in previous DLTS measurements, is believed to be caused by tellurium vacancies.

INTRODUCTION

Cadmium telluride is a direct band gap material, known for its wide use in infrared and γ-ray detectors. With its large bandgap, around 1.5eV, it is also an important candidate for solar energy conversion applications. In addition, it is an ideal substrate for the growth of $Hg_xCd_{1-x}Te$ infrared detectors, because of its close lattice match and chemical compatibility with this material. Several methods, including liquid phase epitaxy (LPE), molecular beam epitaxy (MBE), and organometallic vapor phase epitaxy (OMVPE), have been reported for the preparation of CdTe layers. OMVPE is the most attractive among them for the simplicity of control, lower growth temperature, and the potential of in-situ growth of $Hg_xCd_{1-x}Te$.

Recently, single crystal CdTe grown by OMVPE has been studied for its potential in solar cell applications[1]. However, one of the most important requirements for exploiting this material in photovoltaic devices is to understand and control deep levels in it, since they greatly affect the device performance. In particular, deep levels will limit the minority carrier lifetime and consequently influence the solar cell efficiency. But comparing to the knowledge we have about defects in elemental semiconductors, like Si, and III-V compounds, like GaAs, little is known about deep centers in CdTe. Several research groups have reported DLTS data on bulk materials[2]-[8], while no detail study has been conducted on OMVPE layers.

The goals of the present study are to identify existing deep levels in OMVPE grown CdTe layers, to explore the characteristics of these levels and to investigate the effects of different growth conditions on the deep level concentrations. Thus, this study will provide important feedback to the growth process so that it can be optimized for any devices.

EPITAXIAL GROWTH

The epitaxial growth of CdTe on (100) InSb substrates has been detailed elsewhere[9], and will be summarized here. Growth was carried out at atmospheric pressure in a 51mm I.D. quartz horizontal reactor, using paladium purified hydrogen as the carrier gas. A 25 × 20 × 60 mm. r.f. heated graphite susceptor, was used with the reactor. Substrates were (100) oriented, undoped InSb, prepolished on one side. These were cut into 5 mm × 5 mm in size, cleaned in organic solvents and chemically etched to remove 15-10 μm prior to epitaxial growth. The growth was carried out at a temperature of 420

°C, with a total H_2 flow of 3 *l* /min. The partial pressure of dimethylcadmium (DMCd) was fixed at 1 x 10^{-4} atm and the partial pressure of diethyltelluride (DETe) was varied so that P_{DETe}/P_{DMCd} ranged from 3 to 9. All layers grown were typically 2.5μm in thickness.

After removal from the reactor, gold dots, 0.5 mm diameter and 1000 Å thick, were evaporated on the CdTe surface to form Au-CdTe Schottky barrier diodes.

ELECTRICAL MEASUREMENTS

Capacitance-voltage (C-V) characteristics of the Schottky diodes were measured at room temperature with a PAR-410 C-V plotter in order to obtain the carrier concentrations. The DLTS measurement setup used in the present work, which includes a PAR-410 C-V plotter and dual-gated boxcar averager, is based on the system originally proposed by Lang[10]. The diode temperature was scanned from 100 to 390 K at a rate of about 6 K/min.

The DLTS spectra of CdTe consist of broad and irregular peaks which arise from closely spaced multiple levels. Arrhenius plots and de-convolution techniques were employed to isolate the effect of the separate levels, and to determine their thermal activation energies. For the Au-n-CdTe Schottky diodes under investigation, only electron traps can be detected.

RESULTS

Four different substrates were prepared with P_{DETe}/P_{DMCd} ratio of 3, 5, 7, and 9 (see Table. 1). A number of diodes were measured on each of these substrates. Here we present data on representative samples. The dependence of carrier concentration was obtained from the C^{-2}-V plot at room temperature. Figure 1 shows the dependence of the carrier concentration on P_{DETe}, while P_{DMCd} was kept constant. Since all growth runs considered here were made at a single temperature (420 °C), this figure also represent the dependence of the carrier concentration on P_{Te} with P_{Cd} constant, to a factor of proportionality.

A wide variety of DLTS spectra are observed on these samples. However, all of them can be fitted with a sequence of 5 levels, labelled as E1, E2, E3, E4, and E5. Figure 2 shows the spectra of different samples, together with their separate components. These spectra were taken with a rate window τ^{-1} = 80.47 sec^{-1} and a forward bias pulse width t_f = 10 ms. There was no change in the DLTS peak heights for all the levels when the forward bias pulse width was varied from 5 ms to 70 ms. This indicates that all the levels are completely filled with electrons within 5 ms of application of the pulse.

Table 2 lists the thermal activation energies along with capture cross sections of the five deep levels encountered in this study. Table 3 lists the free electron concentrations, as well as the deep level concentrations of the various levels on different samples. The level E1 was only observed in one sample (NT-233). On the other hand, the levels E2-E5 appeared in all the samples.

DISCUSSION

Like that in III-V compounds, native defects in CdTe play important roles in determining material properties. Several studies have reported them to be the major defects involved in bulk and epitaxial CdTe materials[11][12]. They act as donors or acceptors, they form different kinds of complexes with impurities, and they affect the dopant incorporation in the material.

One of the essential features of the native defects in compound semiconductors is their strong dependence on the availability of the associated reactants during the growth process. For instance, in our case, the concentration of the vacancies, either the cadmium or the tellurium vacancies, depends on the partial pressures of both reactants, DETe and DMCd. A raise of P_{DETe} will result in a reduction of tellurium vacancies as well as an increase of cadmium vacancies. The reason for this can be qualitatively illustrated with a simplified thermodynamic analysis as followed. The dissociation reaction of CdTe can be expressed as

$$CdTe = Cd(g) + 1/2\ Te_2(g) \qquad (1)$$
$$Te_2(g) = 2\ Te(g)$$

Hence

$$P_{Cd}P_{Te} = \text{constant} = K1$$

Furthermore, the formation of neutral cadmium and tellurium vacancies proceeds according to

$$Cd(s) = Cd(g) + V_{Cd}^{o}$$

$$Te(s) = 1/2\ Te_2(g) + V_{Te}^{o}$$

so that

$$[V_{Cd}^{o}]P_{Cd} = K2$$

$$[V_{Cd}^{o}] = (K2/K1)\ P_{Te}$$

and

$$[V_{Te}^{o}] = K3/P_{Te}$$

$$[V_{Te}^{o}] = (K3/K1)\ P_{Cd}$$

Therefore, a change in the partial pressure of one reactant will affect both kinds of vacancies, though in different directions.

On the other hand, the incorporation of interstitials does not follow the chemical reaction of Eq.(1), and the number of interstitial sites available is extremely large. Hence the concentration of interstitials, to an approximation, should be directly proportional only to the partial pressure of the related reactant. Therefore, in our case, we would expect the cadmium interstitials to be relatively independent of the change in P_{DETe}, with P_{DMCd} being held constant. This growth condition dependence provide important information when one tries to determine the causes of native defects.

One interesting point we have observed in the study is the increase of all deep level concentrations with increasing P_{DETe}. It has been reported that overpressure of P_{DETe} will result in higher growth rate of the epitaxial layer[13]. This enhanced growth rate may have been accompanied by more existing defects.

To demonstrate the dependence of different deep levels on P_{DETe} more clearly, Fig. 3 shows the normalized concentration of each level, with respect to the total defect concentration, under different growth conditions. It is clear that level E5 dominates under lower DETe partial pressure, while E4 becomes prominent when this pressure is increased. Level E2 and E3 do not show apparent dependence on P_{DETe}. These trends can also be readily observed directly from Fig. 2. According to these findings, E5 should be related to tellurium vacancies, E4 could be caused by either cadmium vacancies or tellurium interstitials, while E2 and E3 may be associated with cadmium interstitials or impurities.

To further examine the origins of these levels, it is helpful to compare our data with those reported in the literature. Fig. 4 shows suggested energy positions for some of the important native defects, based on Refs. (11) and (12). Note that these levels were determined by techniques other than DLTS, such as the thermally stimulated current measurements. Also shown on the figure are possible corresponding levels from other published DLTS studies on bulk or epitaxial materials. Level E4 and E3 in our case corresponds well to the doubly charged V_{Cd}^{-2} and Cd_i^{+2}. The reported capture cross section for V_{Cd}^{-2} is around 3×10^{-14} cm^2, in close agreement with ours. The level E5 at E_c-1.15 ev has not been reported in DLTS measurements before. Judging from its behaviors shown in Fig. 3 and the information listed in Fig. 4, this level is believed to be the tellurium vacancy V_{Te}.

As to level E2, a similar trap located at E_c-0.36ev has been noted by other workers[6][8][14] in indium doped material, but not in undoped sample. In these studies, the capture cross section of this level has been estimated at around 1×10^{-19} cm^2 [8][14]. Our own measurements indicate a value of about 3.39×10^{-18} cm^2. This level may be associated to a complex involving indium.

In our samples, the free carrier concentration is due to indium, which must occupy cadmium lattice sites to be active donors. As mentioned previously, increasing P_{DETe} should result in an increase of V_{Cd}, thus leading to higher indium incorporation into Cd sites and therefore to higher electron concentrations. This explains the resemblance between the electron concentration behavior in Fig. 1 and the V_{Cd} characteristic curve in Fig. 3.

CONCLUSIONS

DLTS measurements were performed to study deep levels in CdTe layers grown by OMVPE on InSb substrates under different growth conditions. Five levels were detected.

Except the common V_{Cd}^{-2} level, two other levels at E_c-0.65eV and E_c-1.15eV were located and attributed to Cd_i^{+2} and V_{Te} defects. The P_{Te} dependence of these levels provided important information about their origins. The reason for the raise of carrier concentration at high P_{Te} is believed to be the increased availability of Cd sites for In incorporation.

ACKNOWLEDGEMENT

The authors would like to thank J. Barthel for technical assistance on this program. This work was sponsored by the Defence Advanced Research Projects Agency (Contract No. N-00014-85-K-0151), administered through the office of Naval Research, Arlington, Virginia; and by the Solar Energy Research Institute (Grant No. ZL-5-04074-2). Additional funds were provided by Agreement No. 751-RIER-BEA-8 from the New York State Energy Research and Development Authority, in the form of a grant from the international Telephone and Telegraph Company, and from an IBM Fellowship to one of the authors (N. R. T.). This support is greatly appreciated.

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Table 1. OMVPE growth conditions of CdTe layers on InSb substrates

Temperature	420°C
Total flow rate	3 *l* / min.
P_{DMCd}	1.0E-4 atm

Sample	P_{DETe} / P_{DMCd}
NT-238	3
NT-233	5
NT-239	7
NT-242	9

Table 2 Thermal ionization energies and capture cross sections of the detected levels

Level	Thermal ionization energy En (eV)	Capture cross section (cm^2)
E1	0.09 ±0.01	1.33×10^{-19}
E2	0.36 ±0.01	3.39×10^{-18}
E3	0.65 ±0.05	3.26×10^{-14}
E4	0.74 ±0.05	2.92×10^{-14}
E5	1.15 ±0.06	8.7×10^{-10}

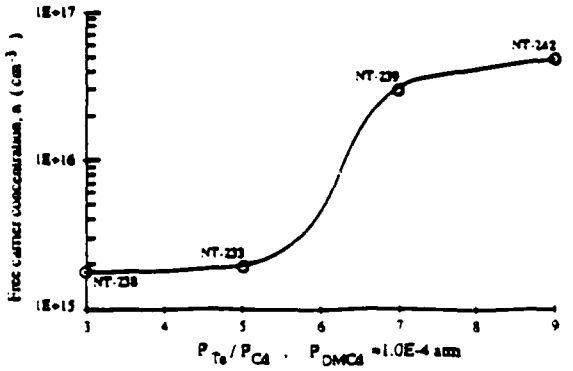


Fig. 1 Dependence of carrier concentration on P_{Te}/P_{Cd} ratio

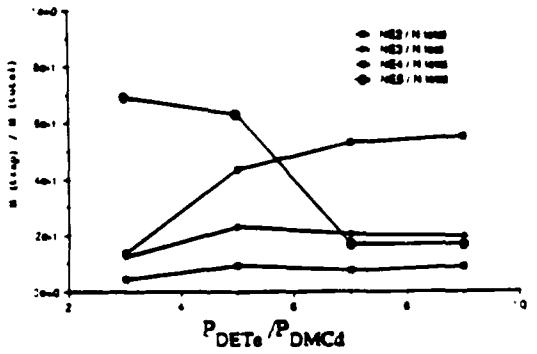
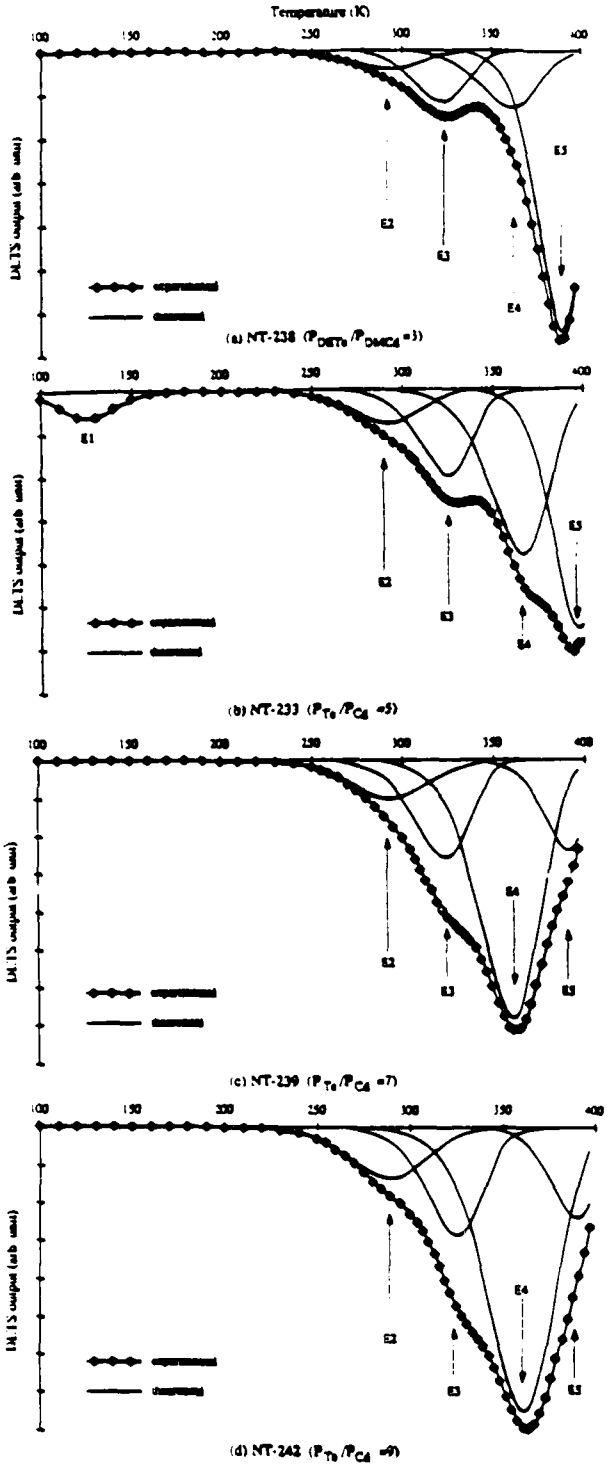


Fig. 3 normalized deep level concentration

Fig. 2. DLTS spectra on different samples



Sample	P_{DETe} / P_{DMCd}	n (cm^{-3})	N_{E1} (cm^{-3})	N_{E2} (cm^{-3})	N_{E3} (cm^{-3})	N_{E4} (cm^{-3})	N_{E5} (cm^{-3})
NT-238	3	1.76×10^{15}	——	2.3×10^{12}	6.6×10^{12}	7.3×10^{12}	3.6×10^{13}
NT-233	5	1.9×10^{15}	1.9×10^{12}	2.4×10^{12}	5.9×10^{12}	1.1×10^{13}	1.6×10^{13}
NT-239	7	3.0×10^{16}	——	4.5×10^{13}	1.2×10^{14}	3.14×10^{14}	1.1×10^{14}
NT-242	9	4.86×10^{16}	——	7.95×10^{13}	1.7×10^{14}	4.83×10^{14}	1.46×10^{14}

Table 3. Free electron concentration and deep level concentration for samples

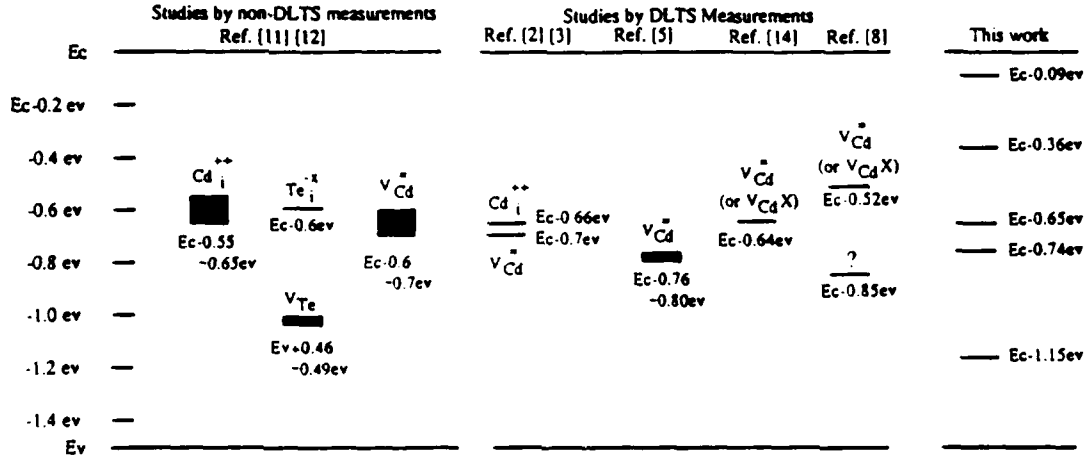


Fig. 4. Important deep levels originated from native defects reported in previous non-DLTS and DLTS Studies. Also shown are the deep levels detected in the present work.

DLTS STUDIES OF N- AND P- CdTe

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SUMMARY:

Deep level transient spectroscopy is used for determining defect levels in n- and p-type CdTe grown by MOCVD technique. In n-type CdTe the defect levels were determined on Schottky diodes. The main majority carrier trap levels were associated to tellurium and cadmium vacancies and cadmium interstitials. PN junctions were used for determining defect levels in p-CdTe where an electron trap and a hole trap were observed.

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I. INTRODUCTION

Cadmium telluride recently has attracted more attention than ever before because of its potential in opto-electronic devices and its lattice compatibility with $Hg_xCd_{1-x}Te$. However, one of the most important requirements for exploiting this material is to understand and control deep levels in it. In this paper, we will discuss the deep centers in cadmium telluride based on the deep level transient spectroscopy (DLTS) technique. Although it is commonly believed that positive identification of a deep center requires extensive information from different experimental measurements, DLTS has certainly been one of the most powerful among them. This sensitive transient measurement technique gives the information of thermal ionization energies, capture cross sections, and concentration profiles of different levels [1]. These are the defect parameters which device engineers are mostly interested in, and which other techniques such as electron paramagnetic resonance (EPR) and photo luminescence (PL) cannot provide. This is one of the major reasons why most of the recent investigations of deep levels in CdTe have utilized this technique.

II. NATIVE DEFECTS IN CdTe

Native defects are always among the most influential deep levels in as-grown or irradiated semiconductors. Common examples of them include vacancies and interstitials. However, there is a kind of defects which exist only in compound materials, i.e. antistructure defects. One well-known example is the level EL2 in GaAs, which is generally attributed to As sitting on Ga sites, As_{Ga}. For binary compounds with similar sized constituents, possibility of the existence of antisite defects is related to the compound ionicity. Formation of antisite defects is less likely in materials with more ionic bonds between constituents since it will be more difficult to exchange atoms on adjacent sites. Van Vechten [2] has calculated the enthalpy of formation for different antisite structures in different compounds, as listed in table 1 and 2. It is seen that formation of antisite defects in II-VI materials is generally much more difficult than that in III-V. This one of the major reasons why no antisite defect has ever been identified in CdTe before.

Since no antisite structure in large concentration is expected in CdTe, vacancies and interstitials become the dominant native defects. Several studies have suggested they be the major deep centers involved in bulk and epitaxial CdTe [3,4]. They can act as donors or acceptors, they can form different kinds of complexes with impurities, and they affect the dopant incorporations. One of the essential features of these native defects in compound semiconductors is their dependence on the availability of constituent elements during growth or annealing. For instance, in the case of vapor phase epitaxial growth, a raise of tellurium partial pressure, P_{Te}, will result in a reduction of tellurium vacancies as well as an increase of cadmium vacancies. Similarly, a raise of

cadmium partial pressure, P_{Cd}, will cause a rise in tellurium vacancies and a fall in cadmium vacancies. On the other hand, incorporation of interstitials, to an approximation, should be directly proportional only to the partial pressure of related component, i.e. $Cd_i \propto P_{Cd}$ and $Te_i \propto P_{Te}$. A change in P_{Cd} alone should not affect the existence of Te_i since the amount of available sites for interstitials is extremely large, and so is the case between P_{Te} and Cd_i. This characteristic of reactant partial pressure dependence can be used to obtain important clues concerning the causes of some deep levels.

III. DEEP LEVELS IN N-CdTe

All of the DLTS characterizations of n-CdTe have been conducted on Schottky diodes [5-14], and hence only electron traps have been reported. Figure 1 summarizes some of the important deep levels detected by different research groups and their possible origins. Also shown in the figure are corresponding levels measured by other techniques [3,4], such as the thermally stimulated current measurements. Another finger-print of deep levels, i.e. electron capture cross section, is not listed here but can be found in the references. Most of these studies were performed on melt-grown bulk CdTe. Heat treatments such as low temperature annealing has been a typical way to investigate the nature of deep levels in these materials. Verity et al. [8] annealed their samples under saturated cadmium pressure with different annealing time, and concluded that increased carrier concentrations with prolonged annealing time is caused by rises in native defects. Collins et al. [9] conducted annealing in hydrogen atmosphere and found drop in both carrier and deep level concentrations, which they suggested to be an indication of some relations between shallow and deep levels. Other researchers

have also conducted annealing in argon or air atmosphere [10,11,13]. They all suggested that deep levels, specially those caused by native defects, will affect the free carrier concentration. However, data from heat treatment experiments should be examined with care since different adverse effects could have obscured the results. For instance, diffusion of contaminants could cause changes of the original deep level nature or doping conditions, and aggregation of defects might create the impression of defect annihilation. It is hard to separate out these effects, which makes it more difficult to draw conclusions from annealing studies under quite different conditions.

As pointed out in the previous section, dependence of deep level concentrations on constituent availability can be used to study the origins of native defects. Takebe et al. [5] has annealed their samples under different cadmium pressures, and were able to find relations between defect concentrations and cadmium partial pressures. Two levels in their study were identified as V_{Cd} and Cd_i from this information. Fig. 2 shows their results of these two levels. Another more reliable approach will be changing the compound composition directly and monitoring the defects in materials with different composition ratios. To achieve this, we have grown CdTe epitaxial layers by OMVPE process under different reactant partial pressures, i.e. P_{DETe} and P_{DMCd}. By doing this we were able to control the availability of the constituent element during growth. Four deep levels noted as E2-E5 were consistently detected in our samples (see Fig. 1) [4]. Three of them are believed to be caused by native defects and have been related to tellurium vacancies (E5), cadmium vacancies (E4), and cadmium interstitials (E3) respectively. Their dependence on growth conditions, as illustrated in Fig. 3, assists our assignment [15]. The origin of E2 is not certain yet, but it could be related to the

dopant, In. Level E5, the tellurium vacancy, was reported for the first time in DLTS characterizations. Our study also indicates incorporation of more defects at higher growth rates [14].

One major deep level detected in most of the DLTS studies is the doubly negatively charged cadmium vacancies. From conventional DLTS derivations, this level is located at about 0.75ev under the conduction band with an electron capture cross section around 3×10^{-14} cm^2, and it should be an electron trap. However, because of its negatively charged state, the electron trap property of this level should be questioned. It has been suggested [6] that this level is a recombination center with an electron capture cross section of 4×10^{-16} cm^2 and a hole capture cross selction of 2×10^{-14} cm^2. This larger capture cross section of holes is more reasonable for a negatively charged state. The consistent appearance of this level is a reflection of the high vapor pressure of cadmium. If this level acts as a recombination center, it is highly possible that it will be one of the most influential deep levels in some devices.

IV. DEEP LEVELS IN P-CdTe

As the case for most semiconductors, the amount of DLTS studies on p-type materials is much less than that on n-materials for CdTe. The small value of hole mobility, and hence large series resistance, of p-CdTe has been an extra obstacle for DLTS characterizations. As far as the authors are aware, there are only two research groups [16,17] which have reported DLTS measurements on p-CdTe. Fig. 4 shows their results, but origins of these levels are still not clear because of the limited information.

We have also performed studies on p-CdTe epitaxial layers grown by

OMVPE process. Measurements were done on n^+-p junction diodes, therefore both electron traps and hole traps can be detected. Initial result shows one major hole trap and one electron trap. Fig. 5 and Fig. 6 are the typical DLTS spectra observed on the sample. From conventional Arrhenius plot scheme, the position of these two levels were found to be 0.59ev above the valence band and 0.58ev under the conduction band respectively. Anomalous behavior was observed for the hole trap. Fig. 6 shows the DLTS spectrum of this level with different filling pulse periods. It seems that complete filling of the hole trap requires a filling pulse of longer than 0.7 seconds, which implies a very slow capture rate. The emission time constant of this level, however, is only about 36ms at 310K, calculated from the boxcar window settings. This fact contradicts the general rule that emission rate of a deep level should be much slower than its capture rate. Possible explanations, such as the field enhanced emission effect, are currently under investigation.

V. CONCLUSIONS

Deep level transient spectroscopy (DLTS) technique has been proven as a powerful tool to investigate deep levels in CdTe. Besides unveiling existing deep centers, it has also provided important information concerning the origins and effects of them in CdTe. Most of the major deep centers are related to native defects. Since antisite structures are not expected to exist in large concentrations, vacancies and interstitials become the main sources of them. A more complete spectrum of deep levels in n-material has been established. However, compared to our knowledge of defects in Si and GaAs, there is still much to be explored in CdTe.

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Legends to Illustrations

Fig. 1. Important deep levels originated from native defects reported in previous non-DLTS and DLTS Studies. Also shown are the deep levels detected in the present work.

Fig. 2. Dependence of concentrations of V_{Cd} and Cd_i on P_{Cd} during the annealing and on the cooling process [5].

Fig. 3. Normalized concentration of E2-E5 as a function of P_{DETe} with P_{DMCd} being fixed. The theoretical curves were derived from thermodynamic analysis. [15].

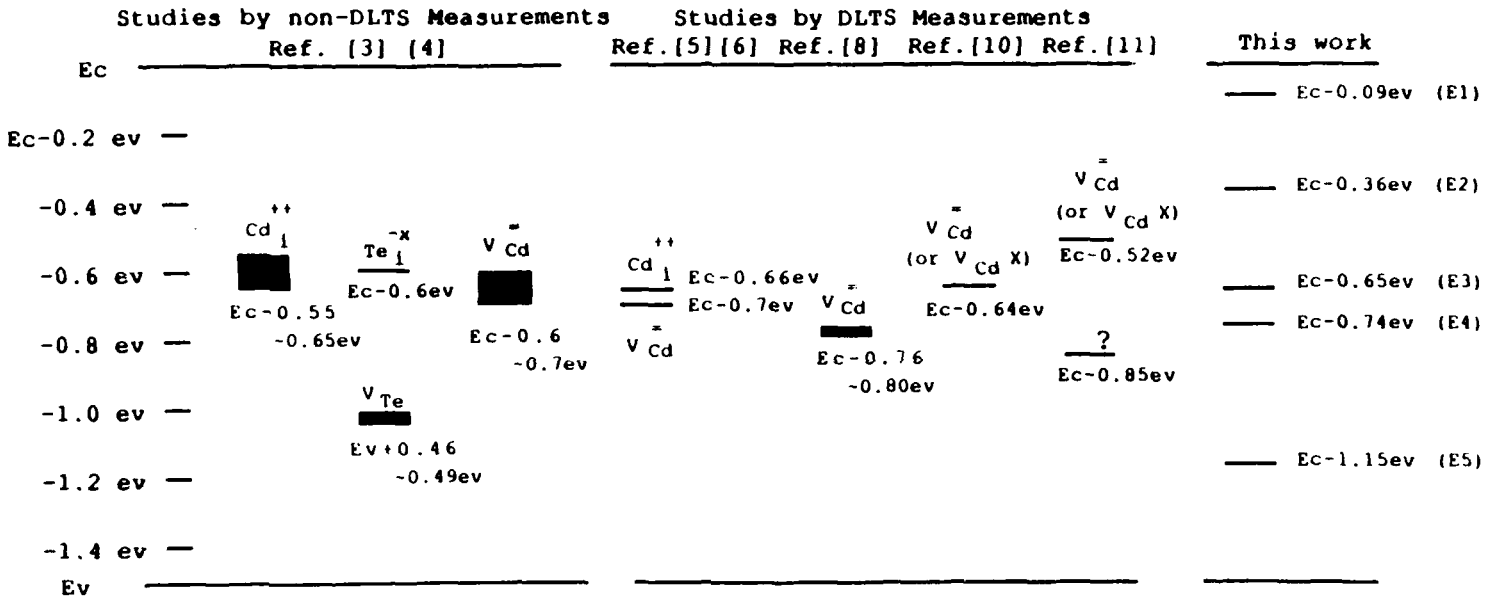
Fig. 4. Arrhenius plots for deep levels detected by R. T. Collins et al. (CH1-CH4) [16] and J. J. Shiau et al. (SH) [17].

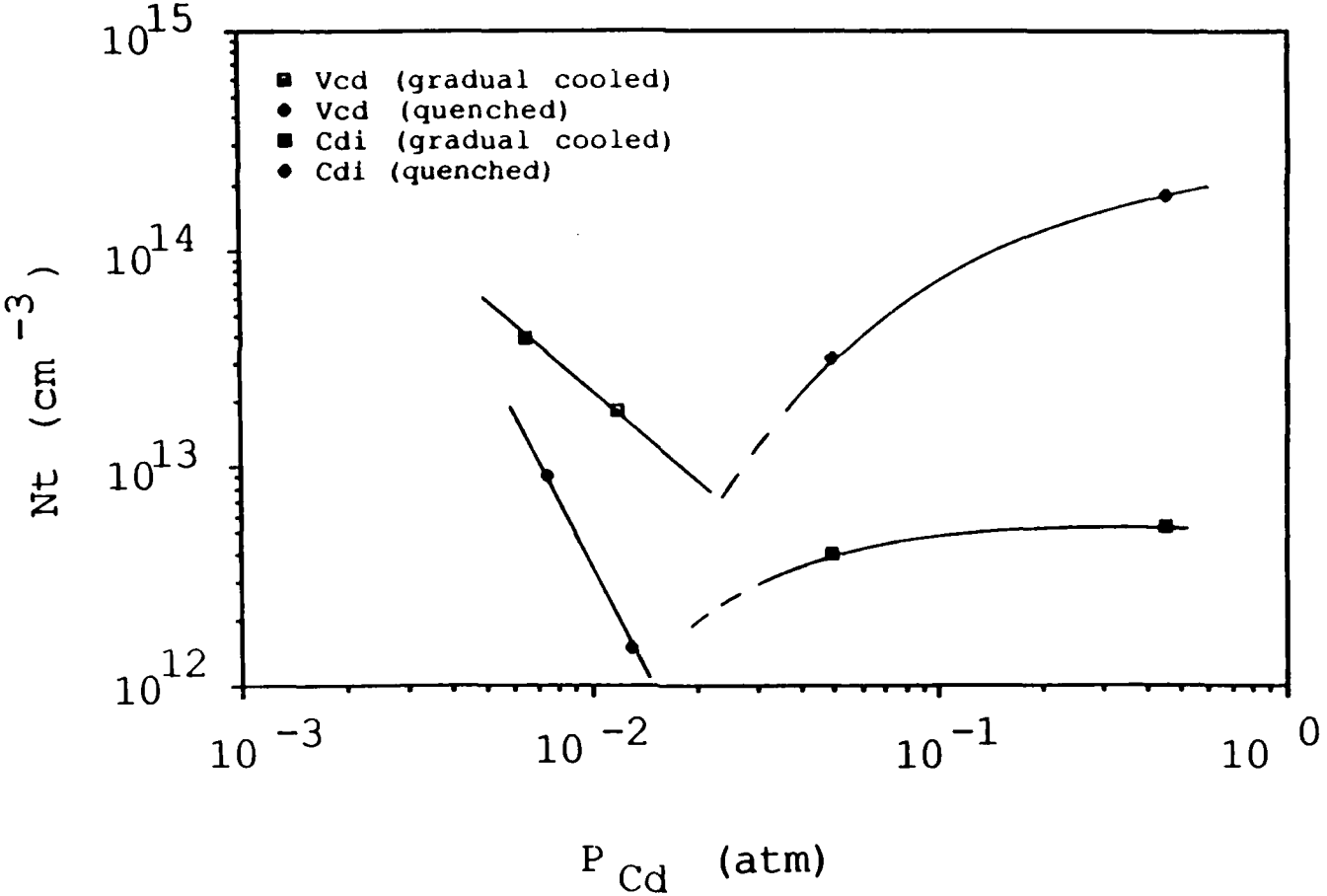
Fig. 5. Electron Trap in p-CdTe (steady state reverse bias 1V, pulse height 2V, rate window 28.85ms).

Fig. 6. Variation of DLTS peak heights for the hole trap in p-CdTe with different pulse width. (steady state reverse bias 5V, pulse height 5V, rate window 36ms).

crystal (AB)	$\Delta Ho(B_A)$ (ev)	$\Delta Ho(A_B)$ (ev)	crystal (AB)	$\Delta Ho(B_A)$ (ev)	$\Delta Ho(A_B)$ (ev)
BN	1.37	0.61			
AlP	0.5	0.60			
GaAs	0.35	0.35	ZnSe	1.25	1.25
InSb	0.27	0.27	CdTe	0.94	0.94

crystal (AB)	$\Delta H(B_A A_B)$ (ev)	crystal (AB)	$\Delta H(B_A A_B)$ (ev)
BN	1.98		
AlP	1.11		
GaAs	0.70	ZnSe	2.51
InSb	0.54	CdTe	1.87


Studies by non-DLTS Measurements
Ref. [3] [4]
Studies by DLTS Measurements
Ref.[5][6] Ref.[8] Ref.[10] Ref.[11]
This work
Ec
Ec-0.2 ev
-0.4 ev
-0.6 ev
-0.8 ev
-1.0 ev
-1.2 ev
-1.4 ev
Ev
Cd i ++
Ec-0.55
~0.65ev
Te i -x
Ec-0.6ev
V Cd =
Ec-0.6
~0.7ev
V Te
Ev+0.46
~0.49ev
Cd i ++
Ec-0.66ev
Ec-0.7ev
V Cd =
V Cd =
Ec-0.76
~0.80ev
V Cd =
(or V Cd X)
Ec-0.64ev
V Cd =
(or V Cd X)
Ec-0.52ev
?
Ec-0.85ev
Ec-0.09ev (E1)
Ec-0.36ev (E2)
Ec-0.65ev (E3)
Ec-0.74ev (E4)
Ec-1.15ev (E5)


Vcd (gradual cooled)
Vcd (quenched)
Cdi (gradual cooled)
Cdi (quenched)
10^{15}
10^{14}
10^{13}
10^{12}
Nt (cm^{-3})
10^{-3}
10^{-2}
10^{-1}
10^{0}
P_{Cd} (atm)

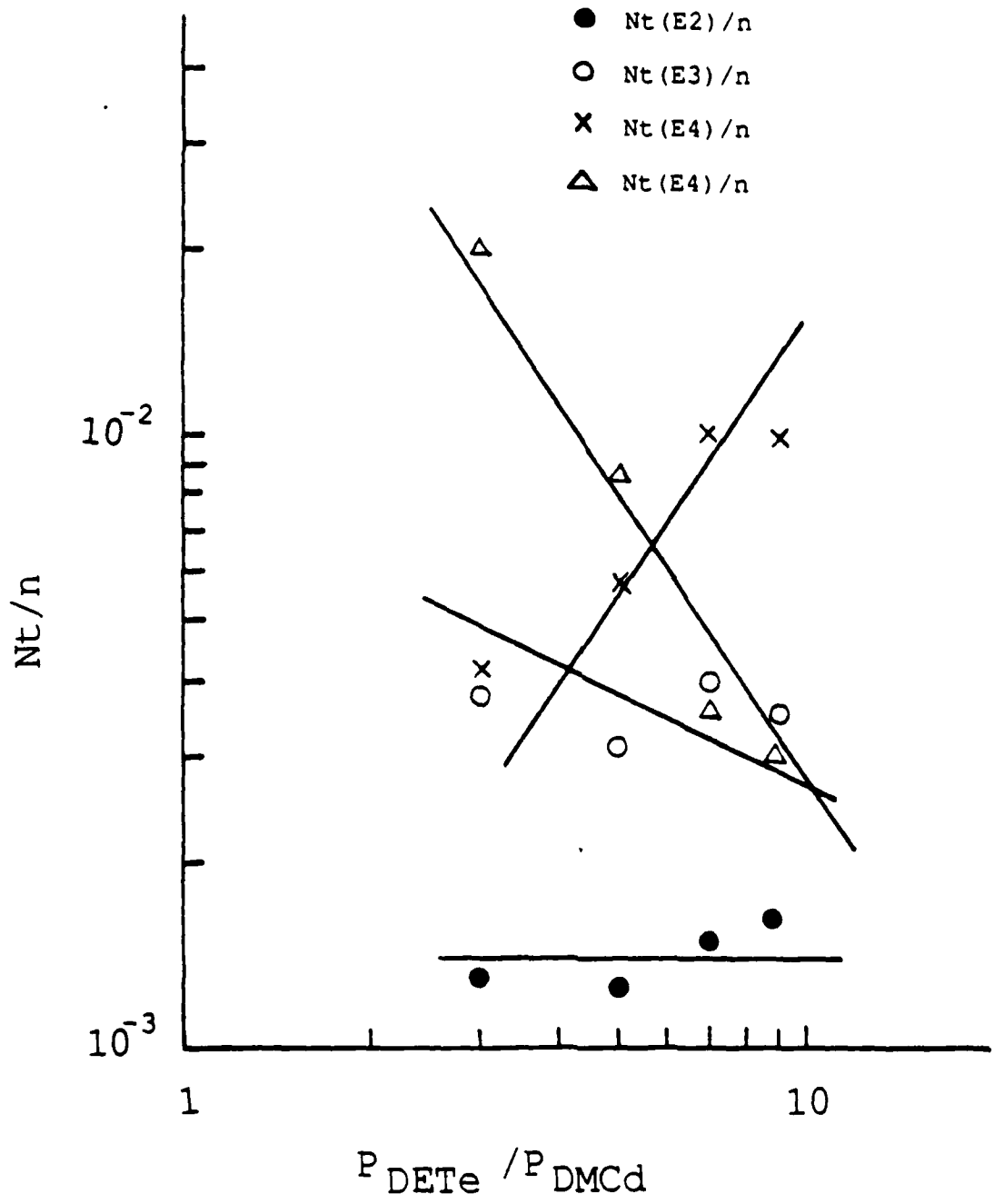


Fig. 3

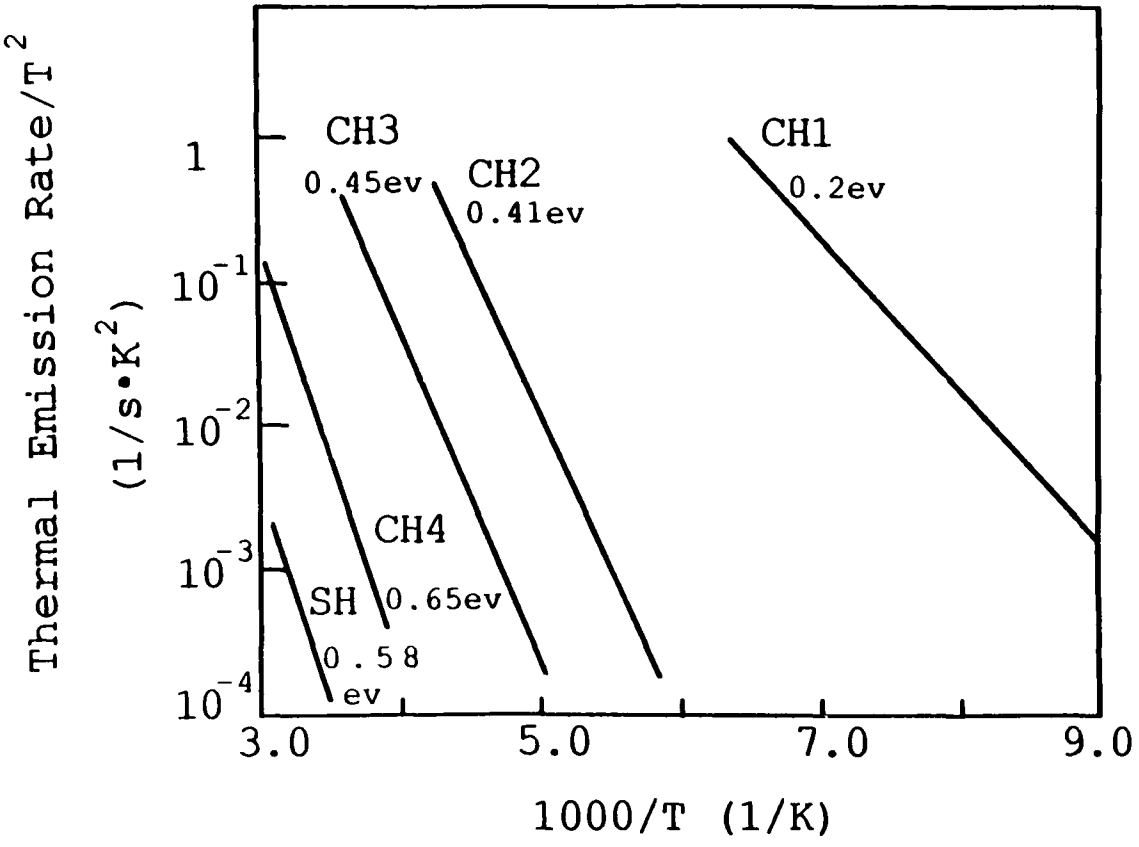

Thermal Emission Rate/T^2
(1/s•K^2)
1
10^{-1}
10^{-2}
10^{-3}
10^{-4}
CH3
0.45ev
CH2
0.41ev
CH1
0.2ev
CH4
0.65ev
SH
0.58
ev
3.0
5.0
7.0
9.0
1000/T (1/K)

Fig 4

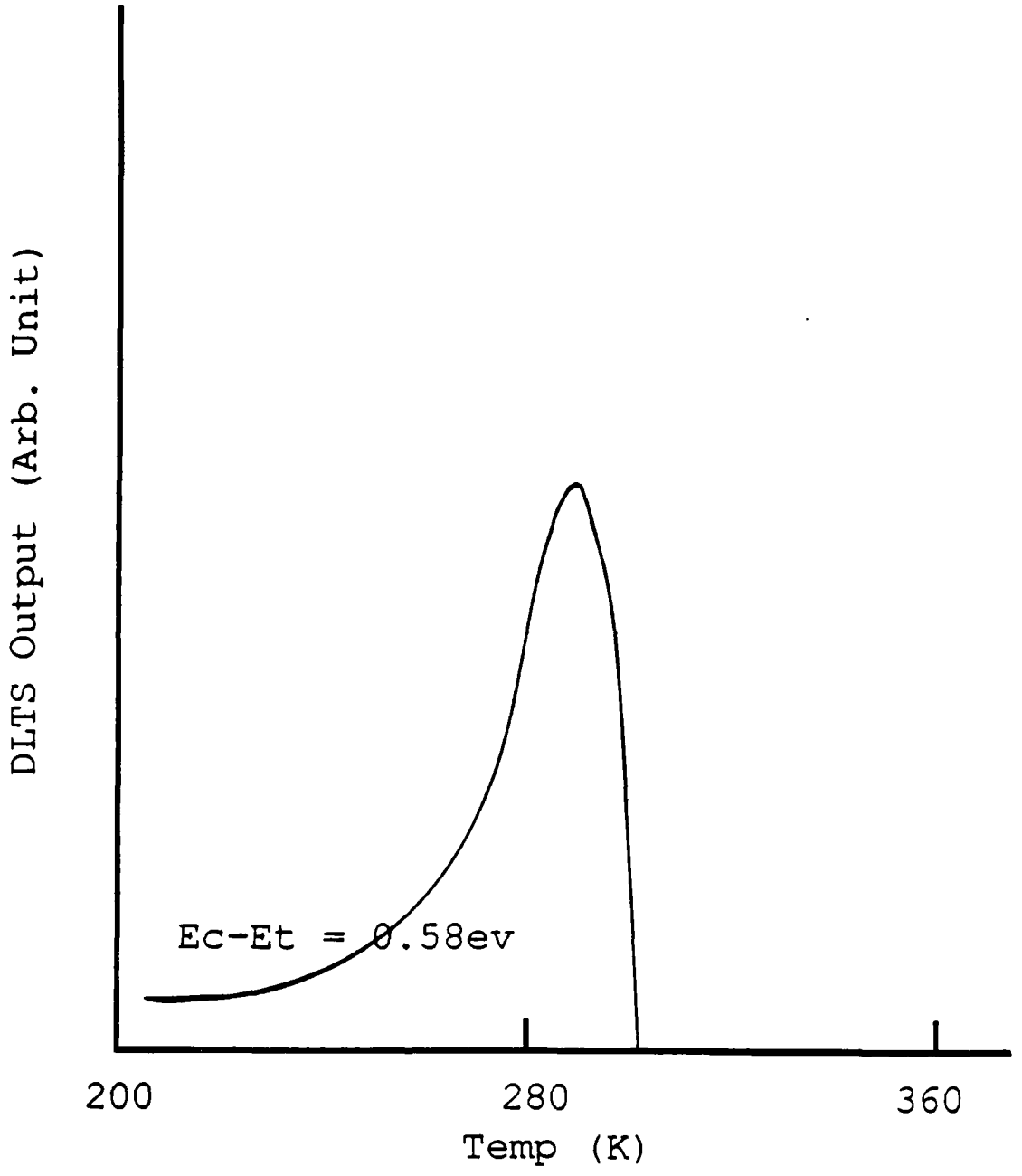


Fig. 5

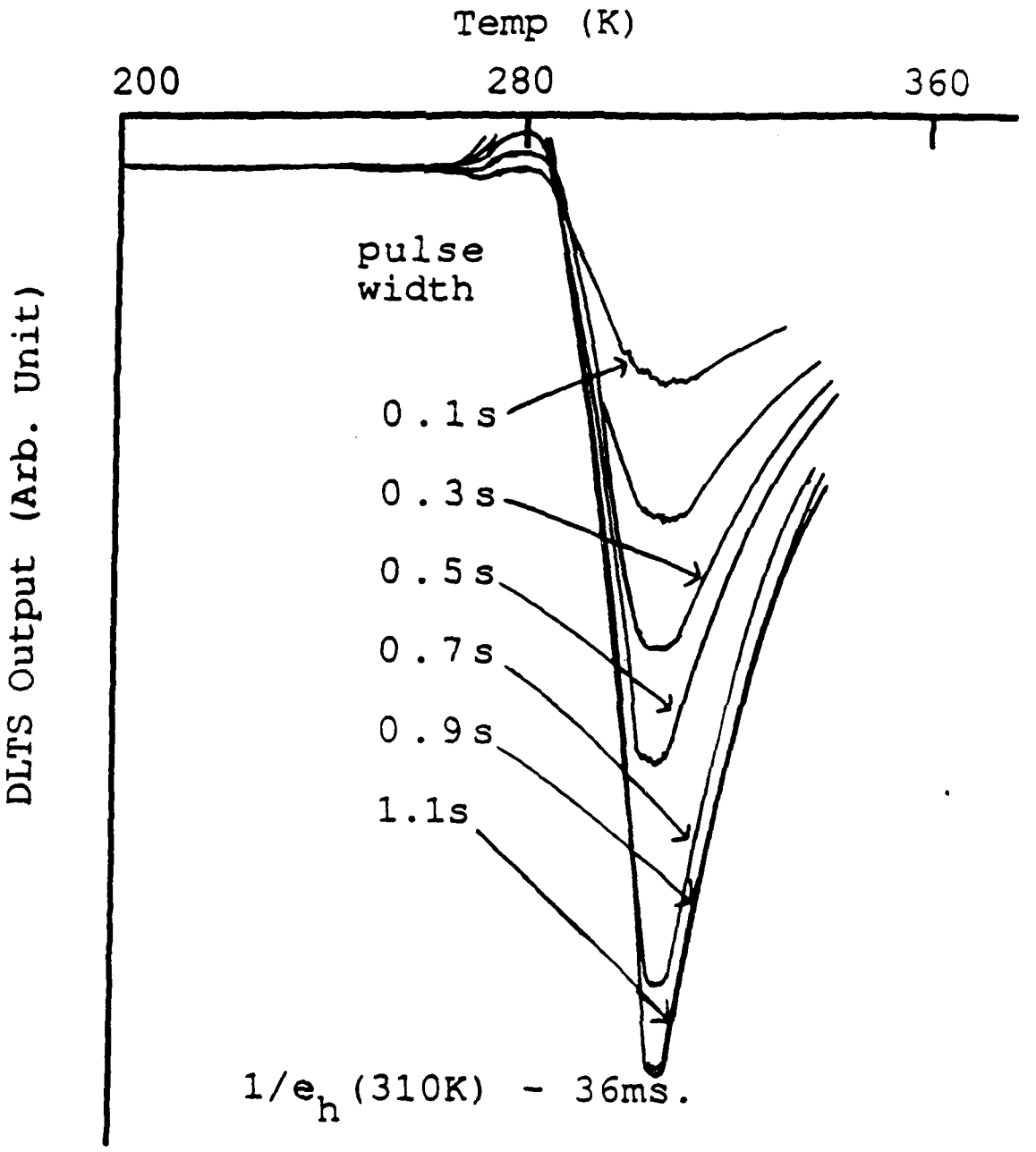

Temp (K)
200
280
360
DLTS Output (Arb. Unit)
pulse
width
0.1s
0.3s
0.5s
0.7s
0.9s
1.1s
1/e_h (310K) - 36ms.
Et-Ev = 0.59ev

Fig. 6

IMPROVED PHOTOLUMINESCENCE OF GaAs IN ZnSe/GaAs HETEROJUNCTIONS GROWN BY ORGANOMETALLIC EPITAXY

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ABSTRACT

Zinc selenide layers, grown by organometallic vapor phase epitaxy on gallium arsenide, are shown to improve the photoluminescence intensity of the Gallium Arsenide. The improvement in the room temperature photoluminescence intensity is found to be as high as 190, for n-type GaAs covered with an 1100 $\AA$ ZnSe layer. An improvement of 145 was observed for p-type GaAs covered by a ZnSe layer of the same thickness. No such improvement is seen for ZnSe thicknesses exceeding 1500 $\AA$, the calculated critical thickness for this heterojunction. The effective recombination velocity is estimated to be approximately 1×10^3 cm/s for the GaAs-ZnSe interface, with thin ZnSe layers. Different epitaxial structures were used to check the consistency of the calculations, and the results match reasonably well.

Our findings suggest that the behavior of the ZnSe/GaAs heterojunction is similar to the AlGaAs/GaAs heterojunction. This presents the possibility of its use in GaAs devices, where it should offer some advantages over the existing structures using AlGaAs.

INTRODUCTION

Many studies of the surface properties of GaAs [1, 2] have shown that its surface recombination velocity (SRV) is very high, approximately 4×10^6 cm/s. This has a detrimental effect on the functioning of surface oriented devices. Various attempts to reduce the SRV using anodic oxides [3], photochemical treatments [4], and other insulating materials [5], have been reported. The AlGaAs/GaAs heteroface has been found to have good interface properties, with SRVs of 1×10^3 to 1×10^4 cm/s, and is extensively used in solar cells and lasers for this reason. The relative instability of high Al containing AlGaAs, and the relatively low bandgap limit the use of this structure. Recently it has been reported that the use of Na_2S film on GaAs leads to improved surface properties [6, 7] of the GaAs. However, this material is water soluble, so that its long term behavior is of concern.

Zinc selenide, which is lattice matched to GaAs (within 0.25%), has been reported to reduce the electric field at the GaAs interface [8] when grown by molecular beam epitaxy (MBE). Here, we report for the first time, the improvement in photoluminescent properties of GaAs using pseudomorphic ZnSe layers grown by organometallic vapor phase epitaxy (OMVPE).

EXPERIMENTAL

For the purpose of this study, GaAs epitaxial layers, of thickness 2-5 μm, were grown [9] by OMVPE using trimethylgallium (TMG) and AsH_3. The nominally undoped layers were 3×10^{15} cm^{-3} n-type. Zn-doped p-type layers with 2.5×10^{15} cm^{-3} doping were also used. Layers were grown on Cr-doped semi-insulating GaAs and on isotype heavily doped substrates, and their results compared in order to isolate the effect of the layer-substrate interface.

Zinc selenide epitaxial layers were grown in a separate, low pressure, OMVPE reactor. Dimethylzinc (DMZ) and dimethylselenide (DMSe) were used for the growth with

ultra high purity hydrogen used as the carrier gas. The total pressure during growth was approximately 200 torr, at a susceptor temperature of 450°C, with a total gas flow of 88 sccm. THe surface temperature of the GaAs was measured as 400°C for these flow conditions. The partial pressure of DMZ was 0.6 torr, while the partial pressure of DMSe was 1.0 torr. The samples were preheated in H_2 to 325°C and held for five minutes at this temperature. A selenium overpressure was used during further heating, and while cooling the samples down to 150°C. Layers from 800 $\AA$ to 1800 $\AA$ were grown, with a growth rate of about 0.17 μm/hr. The ZnSe layer thickness was measured using a multiple beam interferometer.

The photoluminescence (PL) system consisted of a 20 mW Ar-ion laser, a 3/4 m grating spectrometer, and photomultiplier with a liquid nitrogen cooled S-1 photocathode. PL spectra were recorded as a function of temperature from 300K-10K. PL spectra from the GaAs layers were recorded prior to ZnSe growth. After the growth, a part of the sample was covered with black wax and the sample dipped in H_2O_2 to etch the ZnSe from the remaining area, exposing the GaAs below. PL measurements were then taken from both the ZnSe-covered area and the exposed GaAs.

RESULTS

It was found that the PL intensity from the GaAs with the ZnSe cap removed was almost identical to that of the as-grown GaAs epitaxial layer. This, however, should not be taken as conclusive evidence for unchanged properties of the bare GaAs. It is possible that the surface properties (for example, the nature of the surface states) are modified considerably without affecting the PL intensity [10].

Figure 1 compares the PL intensity obtained from the ZnSe-capped GaAs to that obtained from an area where the ZnSe was etched away. Here, the GaAs was n- type, on an n^+ substrate. The shape and the FWHM of the spectra are essentially the same, but the intensity changes considerably. We therefore compared only the maximum inten-

sity values. The ratio $PL_{ZnSe/GaAs}/PL_{GaAs}$ is taken to be indicative of good interfacial properties of the ZnSe/GaAs heterojunctions. This ratio was found to be as high as 190 at 300K. Similar experiments, using p-p^+ GaAs, resulted in a PL improvement of 140 at 300K. The laser chopping frequency was varied between 90 Hz to 4000 Hz, with no change in these improvement factors.

Structures used in the experiments are described in Table I along with the PL ratios at 300K. It has been reported that ZnSe layers with thickness up to 1500 $\AA$, can grow coherently on GaAs [11]. Case 1-3 in Table I are for ZnSe layers with thicknesses less than this critical value. Here, it is seen that the intensity for the ZnSe-capped GaAs is higher than that of the GaAs by a factor of about 100-190. Case 4 in the table is for a ZnSe layer of thickness about 1800 A; here the intensity ratio was found to be only 1.5. We propose that this layer has relaxed by the introduction of misfit dislocations, with a resultant deterioration of its interfacial properties, accompanied by an increase in the interfacial recombination velocity.

Case 1 and 2 are for two similar n-type epitaxial layers, grown on n^+-GaAs and semi-insulating GaAs substrates respectively. This permits us to change the back SRV, while the front SRV remains unaffected, and allows a check on front SRV calculations for consistency.

DISCUSSION

The PL intensity from a sample is proportional to the total number of excess carriers generated. The excess charge associated with these carriers can be calculated by solving the continuity equation with appropriate boundary conditions. We have used the procedure of Duggan and Scott [12], who have solved these equations for an epitaxial layer with front and back surface recombination velocity (SRV) taken into account. However, as our epitaxial layer thicknesses (d) are relatively small, the correction due to reabsorption of PL is about 5%, and has been ignored. Here it should be pointed out

that these calculations assume no band bending and therefore give values of an effective SRV.

The estimation of effective SRV for the GaAs/ZnSe heterojunction was carried out [12], using the values given in Table II. By this means, the estimated front SRV is approximately 1-2 $\times$ 10^3 cm/s. In the case of the p/p^+ GaAs, (Case 3 in Table I), the observed improvement ratio was 145, comparable to the n/n^+ case. Assuming a back SRV of 2 $\times$ 10^3 cm/s, we estimate the front SRV to be 1.5 $\times$ 10^3 cm/s. This result implies that the observed intensity improvement caused by the ZnSe layer is not related to some surface field alone, but results from improved interfacial properties.

In order to see the effect of temperature, PL measurements were made in the range 10K to 300K. Figure 2 shows that the PL spectra taken from ZnSe capped and bare GaAs were identical in shape at all temperatures. The ratio of the intensities was, however, found to change. In the temperature range 300-250K, the ratio remains approximately constant. However, between 250K-150K, the ratio falls with the temperature. The exact nature of this variation is due to the temperature dependence of factors such as the SRV, diffusion of carriers away from the surface, and the radiative and non-radiative components of the bulk lifetime. Below 150K, the ratio falls marginally.

CONCLUSION

It has been shown that pseudomorphic layers of ZnSe on GaAs lead to a significant improvement in the PL intensity of GaAs. The effective interfacial recombination velocities for the ZnSe/GaAs heterojunctions are estimated to be about 1-2 $\times$ 10^3 cm/s. This presents the possibilities of using ZnSe layers in GaAs devices such as solar cells and in some laser structures.

ACKNOWLEDGEMENT

The authors would like to thank J. Barthel for technical assistance on this program, and P. Magilligan for manuscript preparation. This work was sponsored by the Defense

Advanced Research Projects Agency (Contract Number N-00014-85-K-0151), administered through the Office of Naval Research, Arlington, Virginia; and by the Solar Energy Research Institute (Grant No. ZL-5-05018-2). Additional funds were provided by Agreement No. 970-ERER-ER-87 from the New York State Energy Research and Development Authority. This support is greatly appreciated.

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Case	Epitaxial Structure	Thickness of ZnSe	PL Improvement at 300K
1.	n/n^+GaAs $n = 3 \times 10^{15}\text{cm}^{-3}$ $n^+ = 2 \times 10^{17}\text{cm}^{-3}$ $d = 1.75\mu m$	$1100\mathring{A}$	190
2.	$n/Si\ GaAs$ $n = 3 \times 10^{15}\text{cm}^{-3}$ $d = 1.75\mu m$	$1100\mathring{A}$	100
3.	p/p^+ $p = 2.2 \times 10^{15}\text{cm}^{-3}$ $p^+ \simeq 10^{17}\text{cm}^{-3}$ $d = 3.25\mu m$	$850\mathring{A}$	145
4.	n/n^+GaAs $n = 3 \times 10^{15}\text{cm}^{-3}$ $n^+ \simeq 10^{18}\text{cm}^{-3}$ $d = 3.2\mu m$	$1800\mathring{A}$	1.5

Bulk Lifetime:	$600ns$
Diffusion Length:	$20\mu m$
Front SRV for Native GaAs:	4×10^6cm/s
Back SRV for $n^- - n^+$ GaAs:	2×10^3cm/s
Back SRV for n-Si GaAs:	5×10^3cm/s
Back SRV for $p - p^+$ GaAs:	2×10^3cm/s

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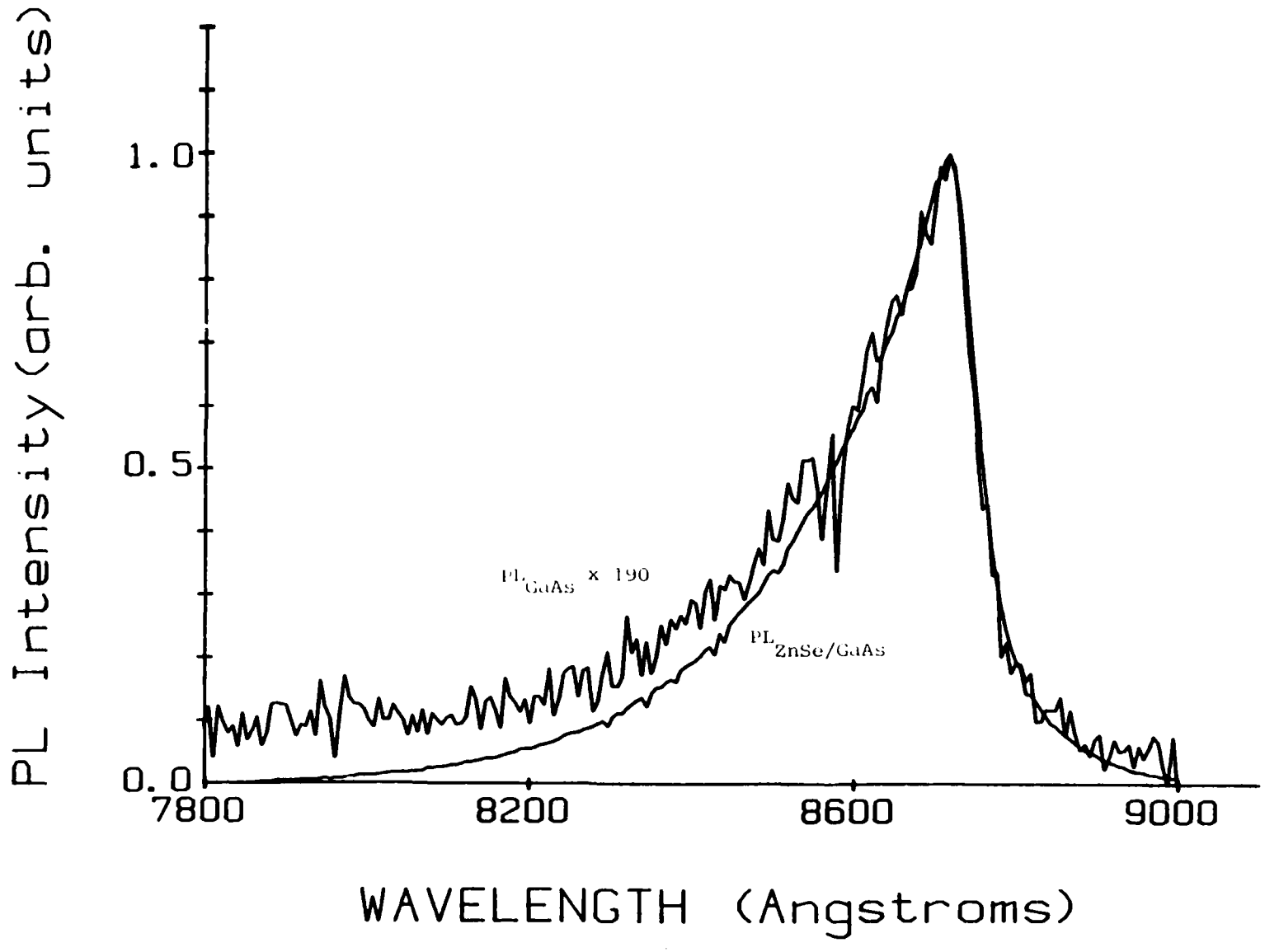
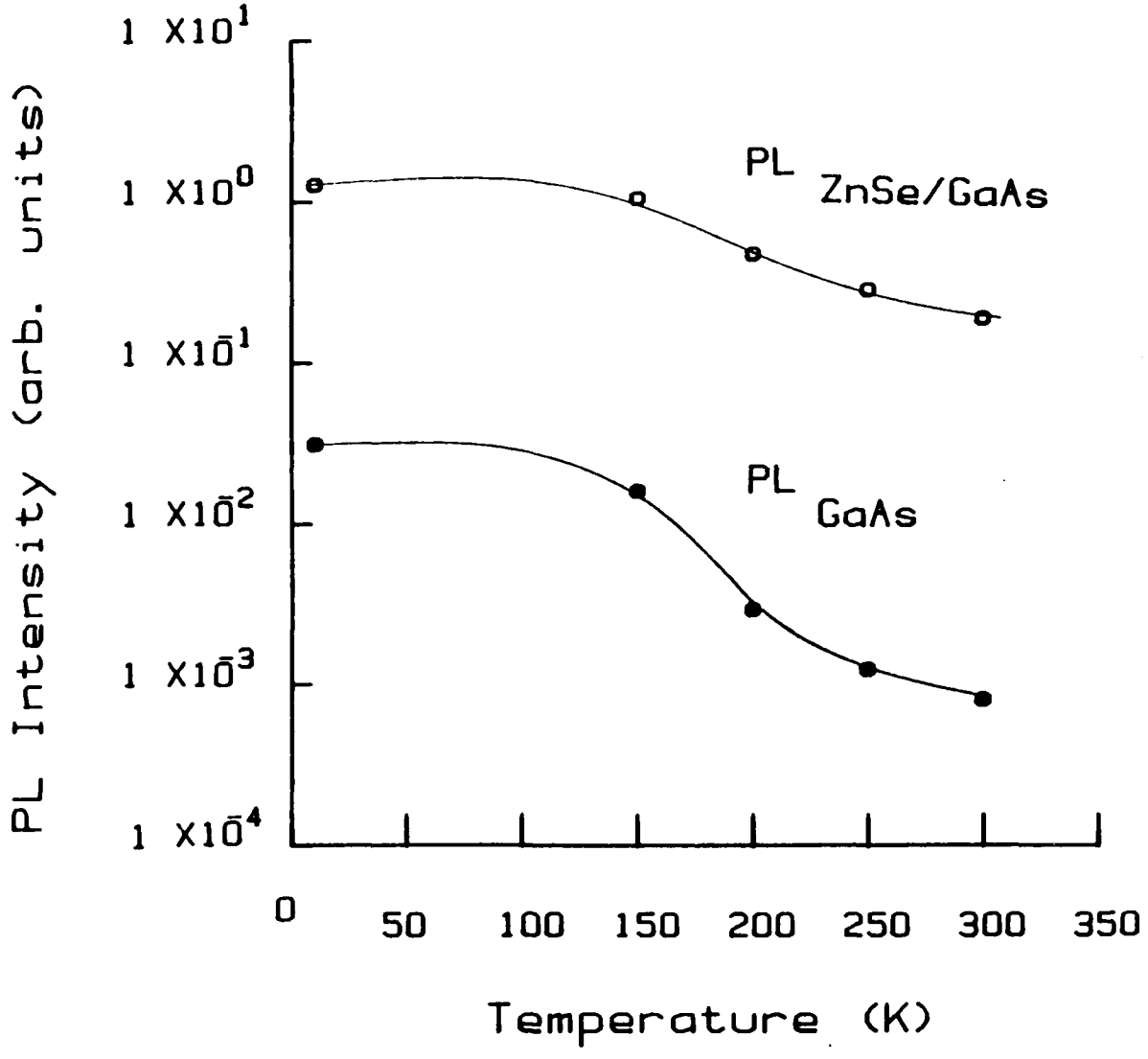

PL Intensity (arb. units)
1.0
0.5
0.0
7800
8200
8600
9000
WAVELENGTH (Angstroms)
PL GaAs x 190
PL ZnSe/GaAs


1 X10^1
1 X10^0
1 X10^-1
1 X10^-2
1 X10^-3
1 X10^-4
PL Intensity (arb. units)
PL ZnSe/GaAs
PL GaAs
0
50
100
150
200
250
300
350
Temperature (K)

GROWTH AND PROPERTIES OF $Hg_{1-x}Cd_xTe$ ON GaAs, WITH $x \simeq 0.27$

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SK-87.15

March 7, 1988

ABSTRACT

The organometallic vapor phase epitaxy of HgCdTe onto (100)2°–(110) GaAs substrates is described in this paper. A buffer layer of CdTe has been grown prior to the growth of HgCdTe, to take up the large lattice mismatch with the GaAs. Considerations for the thickness of this buffer layer are outlined, and it is shown by quantitative Secondary Ion Mass Spectroscopy that there is negligible diffusion of gallium from the GaAs substrate for the growth conditions described. Hall effect measurements give mobilities comparable to those report for bulk grown crystals. An extrinsic n-type carrier concentration of $2 \times 10^{16}/\text{cm}^3$ is obtained, and is mainly due to residual impurities in the starting chemicals.

The alloy composition has been determined by Fourier transform infrared transmission spectrometry, and is found to be extremely uniform over a 15 mm $\times$ 7 mm area. HgCdTe layers have been grown on buffer layers varying in thickness from 0.1 to 1.9 μm. It is found that a buffer thickness of about 1.9 μm or larger is required to obtain high quality HgCdTe, both in terms of the electrical characteristics (mobility and carrier concentration) and the infrared transmission curves (peak transmission).

INTRODUCTION

There is considerable interest in the epitaxy of mercury cadmium telluride (MCT) because of its unrivalled performance in infrared detector applications. Device quality material has been produced by a number of epitaxial growth methods [1-3], with cadmium telluride as a substrate material because of its reasonably good lattice match with MCT over the entire composition range. However, the lack of availability of bulk CdTe with high structural quality has emphasized the need for alternate substrates such as GaAs. An intervening CdTe buffer layer of suitable thickness and crystal quality is required to accommodate the large lattice mismatch (14.6%) that is present between MCT and GaAs.

We have shown that organometallic vapor phase epitaxy (OMVPE) can be used to grow this buffer layer [4] and have presented results on the growth of MCT on GaAs with an intervening semi-insulating CdTe buffer [5]. Here, the previous growth emphasis was on $Hg_{1-x}Cd_xTe$ material with x = 0.2, which is suited for the 10.6 μm range. Higher values of x are required to extend the use of this semiconductor to the shorter wavelength region [6]. In this work, we report on MCT with $x \simeq 0.27$, grown by OMVPE on GaAs substrates, with a buffer layer of undoped, semi-insulating CdTe. The growth process and electrical characteristics of the MCT are described in this paper.

EXPERIMENTAL

The epitaxial reactor used in this study consisted of a horizontal quartz tube with an RF-heated graphite susceptor. All the growth runs were conducted at atmospheric pressure. Palladium purified hydrogen gas was used to transport elemental mercury held at 300°C and the organometallic reactants: dimethylcadmium (DMCd) and diethyltelluride (DETe). The tube wall in front of the susceptor was heated to 230 °C to prevent mercury condensation. The substrates used were (100)2° → (110) semi-insulating GaAs typically 7mm by 7mm in size. These samples were degreased in trichloroethylene, ace-

tone and methanol followed by a 5 min. etch in Caro's etch (H_2SO_4:H_2O_2:H_2O = 5:1:1) to remove the top 10 μm of surface damage. Just prior to loading, they were given a 1 min etch in a solution containing NH_4OH:H_2O_2:H_2O = 10:1:1 by volume. The CdTe buffer layers were grown at 350°C with the DMCd and DETe flows adjusted to obtain a growth rate of 2.5 μm/hr. The thickness of the buffer was varied from 0.1 to 1.9 μm. The MCT layers were grown at a susceptor temperature of 415°C on the CdTe buffer for 90 min, resulting in a layer thickness of 3.0 μm.

The composition and thickness of the MCT layers were determined from the IR transmission characteristics, using a Fourier Transform Infrared (FTIR) spectrometer. Interference fringes that appear in the transmission characteristic at around 10μm were used to calculate the film thickness, assuming a refractive index of 3.4 [7].

Many approaches are used for determining the bandgap, and hence the composition, of the grown layers from optical measurements [7]. Hansen et. al. [8] have given a formulation for E_g at different n and T, by taking E_g to be the energy at which α = 500 cm^{-1}. This corresponds to a suitable cut off energy for 10 μm devices. Recently Chu et. al. [9] have related the high absorption region to the bandgap. The bandgap energy typically corresponds to values of α in the range 3000-4000 cm^{-1}. Their values are uniformly higher than those given by Hansen et. al. but are well corroborated by magneto-optical methods for directly measuring the bandgap. We have used the formulation given in [9] because it is particularly suited to the evaluation of thin epiaxial layers. In our samples, band tailing effects due to high defect doping cause considerable uncertainty in evaluating intrinsic absorption coefficients around 500 cm^{-1} so that the method of Hansen et. al. can lead to considerable error.

Electrical measurements were made by the van der Pauw technique. Since both the undoped CdTe and the GaAs substrate were semi-insulating, clover leaf patterns were delineated in the MCT layer and ohmic contacts were made by soldering indium dots.

A magnetic field strength of 2.1 kG was used for these measurements, which were taken from 300 K to 15 K.

RESULTS AND DISCUSSION

Surface Morphology:

The morphology of these layers as observed under a microscope was very smooth except for the presence of elongated hillocks as shown in Fig. 1. The hillock density was in the range of 4000 to 5000 cm^{-2} for the surface preparation process described earlier. Omission of the ammonia etch step was found to double these values.

The hillocks became more pronounced and bigger in size as the buffer layer thickness was increased. Since the thickness of the MCT layer was the same for all our samples, this indicates that the defects originate at or near the GaAs-CdTe interface. The elongated hillocks were aligned towards a (110) direction, irrespective of the sample orientation on the susceptor, indicating that they might be related to the misorientation plane of the samples.

Buffer Layer Characteristics:

The crystal quality of the CdTe buffer layer, grown on GaAs at 350°C, has been studied by transmission electron microscopy [10]. It was observed that extended dislocation networks, which begin at the CdTe-GaAs interface due to lattice mismatch, do not propagate along 60° glide planes beyond a thickness of about 1.2 μm. Recently, we have done further studies to assess the potential problem of Ga out-diffusion into the CdTe layer. Electrical characterization shows that these layers are undoped and semi- insulating, and quantitative secondary ion mass spectroscopy (SIMS) confirms our results. Figure 2 shows the depth profile of Ga in two CdTe layers grown on GaAs, as obtained by a quantitative SIMS measurement. These measurements were made by Charles Evans and Associates, using oxygen ion bombardment and positive secondary ion mass spec-

trometry. Figure 2(a) shows the SIMS profile of a CdTe layer grown at 350°C. Here, the Ga concentration is seen to fall to the background level within a distance of 0.1 μm from the interface. The increase in Ga concentration near the surface is artifact of the measurement technique.

To simulate the conditions during growth of MCT on a CdTe buffer, a CdTe layer grown on GaAs, and held at 415°C under DMCd overpressure for one hour. The SIMS profile of such a layer, shown in Fig. 2(b), shows that the out-diffusion distance is still very low, with the Ga level falling below $1 \times 10^{15}/\text{cm}^3$ within 0.5 μm of the interface. Thus, Ga doping of the MCT layer can be neglected for buffer layers that are thicker than 1 μm.

Crystal Quality:

Since the CdTe buffer is of good single crystal quality and featureless except for the *hillocks*, we would expect that the MCT layers would also reflect the same crystal quality. This is borne out by the band edge transmittance of a typical MCT layer, as shown in Fig. 3. The presence of the fringes below the MCT bandgap indicate a sharp interface between the substrate and epi-layer. An important feature of the transmittance curve is the peak value of transmission, which should be about 60%, for MCT ($x \simeq 0.27$) on CdTe, assuming ideal layers. However, if the defect and impurity density in the sample is high, there is considerable residual absorption in the pass band region of the MCT. Thus samples with thin buffer layers have a peak transmission of only about 40%. We have noticed that, for buffer layers of 1.9 μm, the peak transmission is 60%, from which we conclude that such MCT layers are reasonably free from defects.

Electrical Characteristics:

The thickness of the buffer layer has a pronounced effect on the electrical properties of the MCT layers. In Fig. 4(a), the 77K Hall mobility is plotted as a function of the

buffer layer thickness for a series of MCT layers, with x = 0.27. We note that the mobility value rises until the buffer thickness is 2 μm, consistent with our earlier observations based on IR transmission. For comparison, the electron mobility (for the carrier concentration obtained by us) for MCT of $n = 0.27$ is indicated in the axis [11]. The trend in mobility is similar to the results obtained for $x = 0.2$ layers, reported previously [5], which is also shown in this figure.

This trend can be explained by examining Fig. 4(b) which gives the electron concentration as a function of the buffer layer thickness. The linear fall- off in scattering centers would cause the 77K mobility, where ionized impurity scattering is relatively important, to increase. The fall in carrier concentration in turn is to be expected if we consider the strain induced migration of Hg interstitials during growth [12]. This causes a strong n-type behavior in the layer, probably because the mercury diffusion occurs via charged defects. The lower limit to this value is set by the residual impurities in the starting chemicals and by the annealing process conditions. We found a value of $2 \times 10^{16}/cm^3$ to be the lowest for our process conditions and confirmed this by the growth of MCT on bulk CdTe substrates. We note from Fig. 4(b) that this value is approached as the buffer layer is made thicker than 1.9 μm.

Figure 5(a) shows the electron mobility as a function of temperature for a 2.9 μm thick MCT layer grown on a 1.9 μm buffer layer. The mobility peaks at a maximum value of 80000 cm^2/V-sec, at about 20K, showing that optical scattering is dominant even at low temperatures. Figure 6(b) shows the variation of the Hall coefficient (= 1/qn) of the same layer with reciprocal temperature. No carrier freeze-out is seen down to 15K, which is to be expected because of the low effective mass, and hence the low donor ionization energy for MCT layers of this composition.

CONCLUSION

We have shown that high quality layers of $Hg_{0.73}Cd_{0.27}Te$ can be grown on GaAs,

provided that the misfit stress is taken up by a sufficiently thick CdTe buffer layer. A consideration of both the optical and the electrical characteristics indicates that the buffer should at least be 1.9 μm thick. With such a buffer, the IR transmission characteristic is near-ideal, and the mobility compares well with values reported for bulk MCT. Quantitative SIMS studies also show that the effects of Ga out-diffusion into the MCT layer are negligible for buffer layer thicknesses above 1 μm. The surface shows the presence of hillocks, whose concentration can be reduced considerably by proper surface preparation.

ACKNOWLEDGEMENT

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11. Data from M.W. Scott in Chap. 1 of Ref. 6.
12. P.M. Raccah and U. Lee, J. Vac. Sci. Technol., A1(3), 1587 (1983).

LIST OF FIGURES

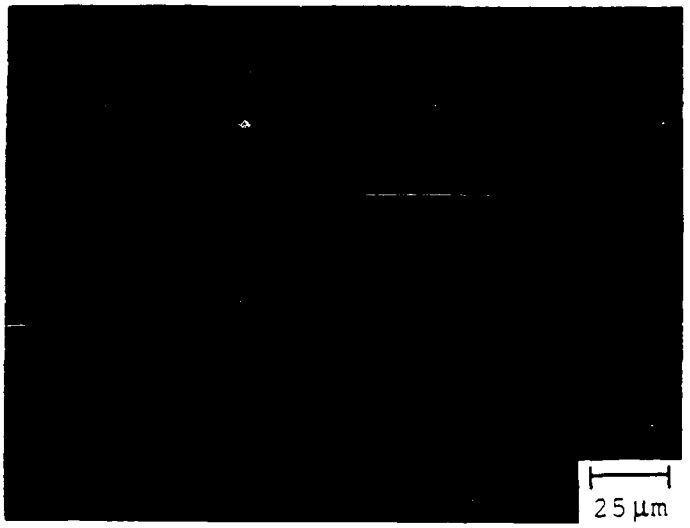

FIG 1

V.N et al

PROCESSED DATA

CHARLES EVANS AND ASSOCIATES

11 Sep 86

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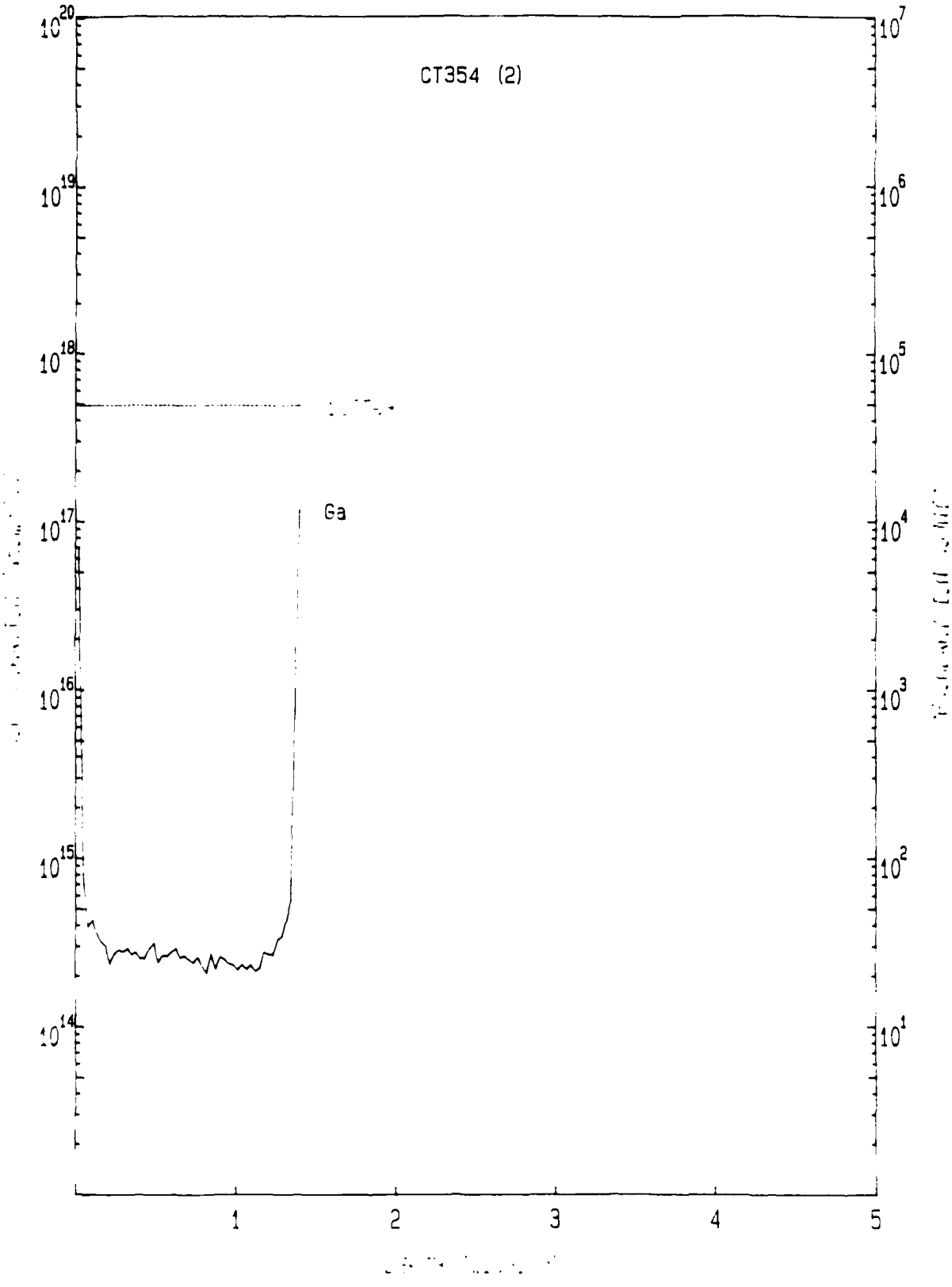

FIG. 2a

V.N et al

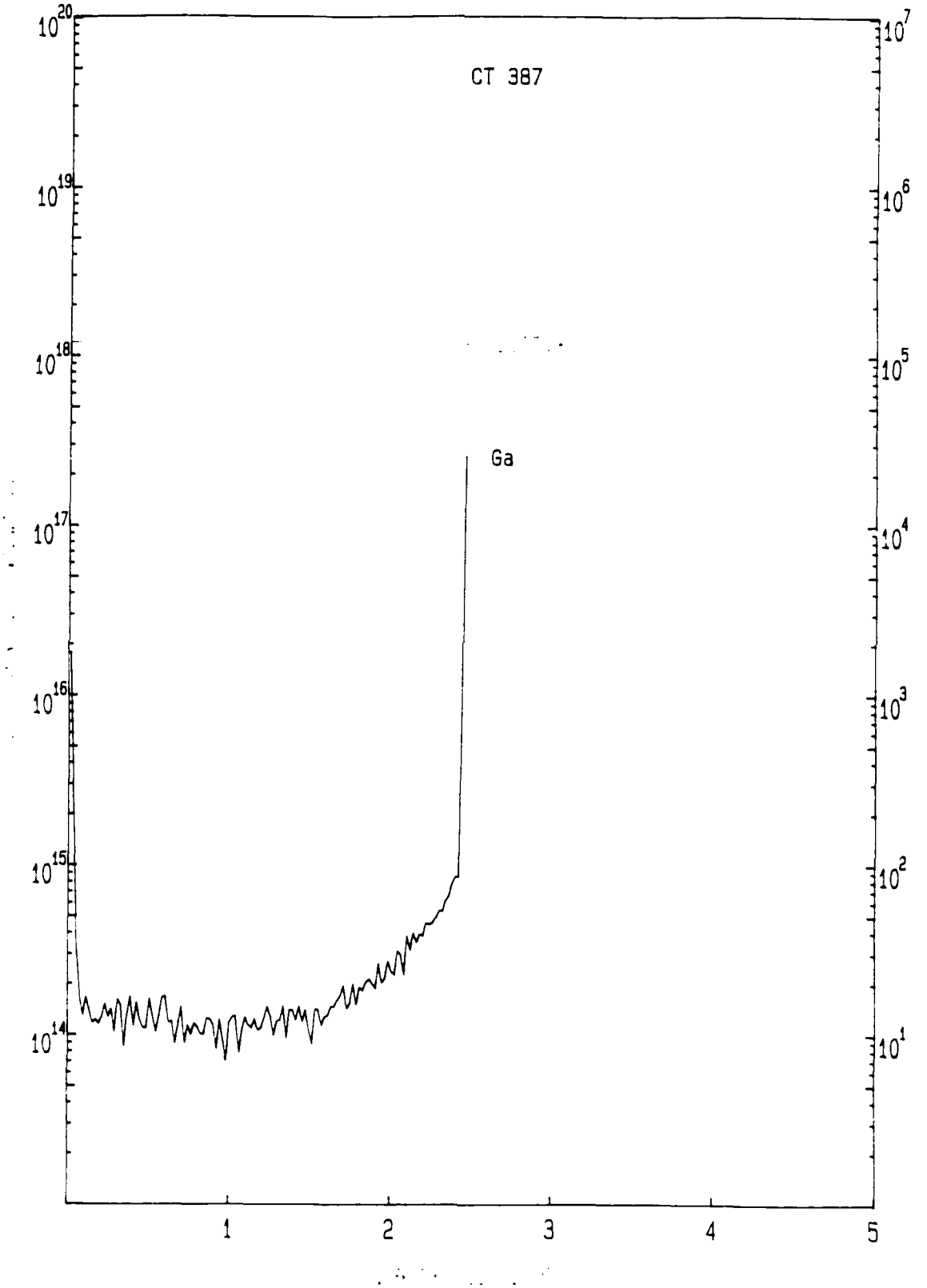

FIG 2 b

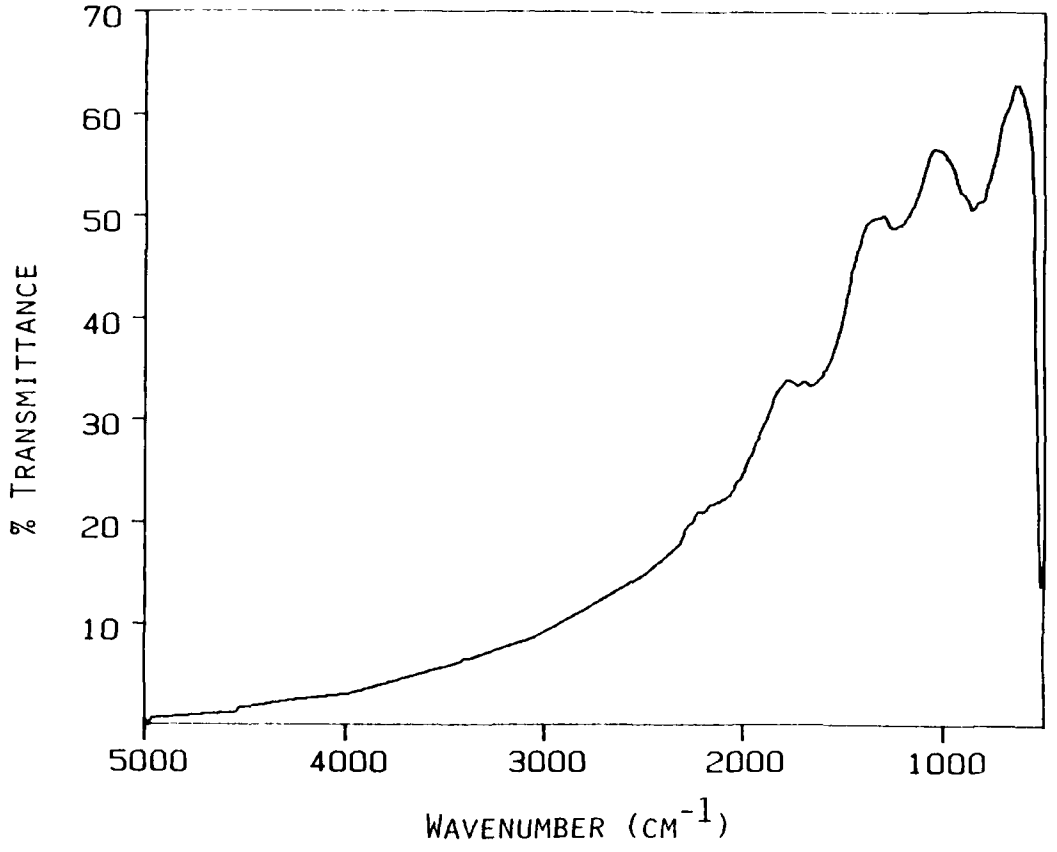
70
60
50
40
30
20
10
% TRANSMITTANCE
5000
4000
3000
2000
1000
WAVENUMBER (CM^{-1})

FIG. 3

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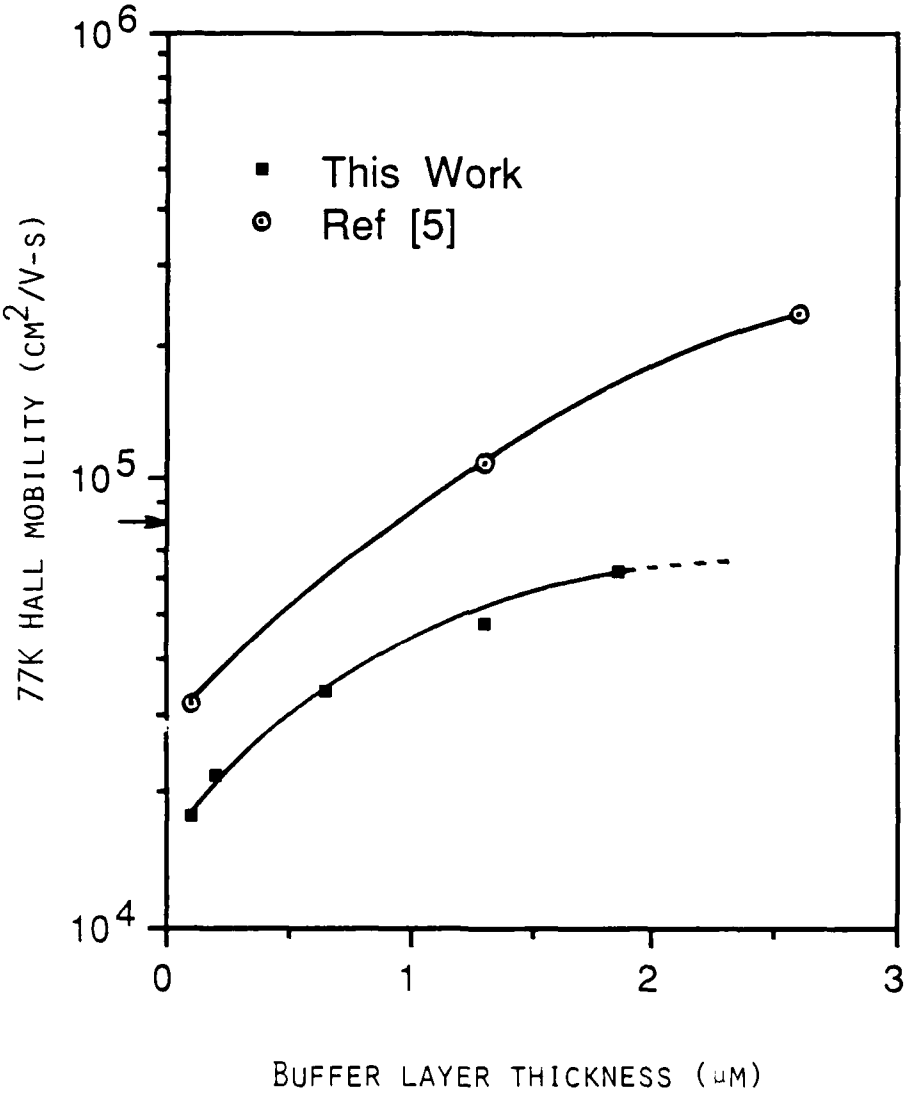

FIG 4 a

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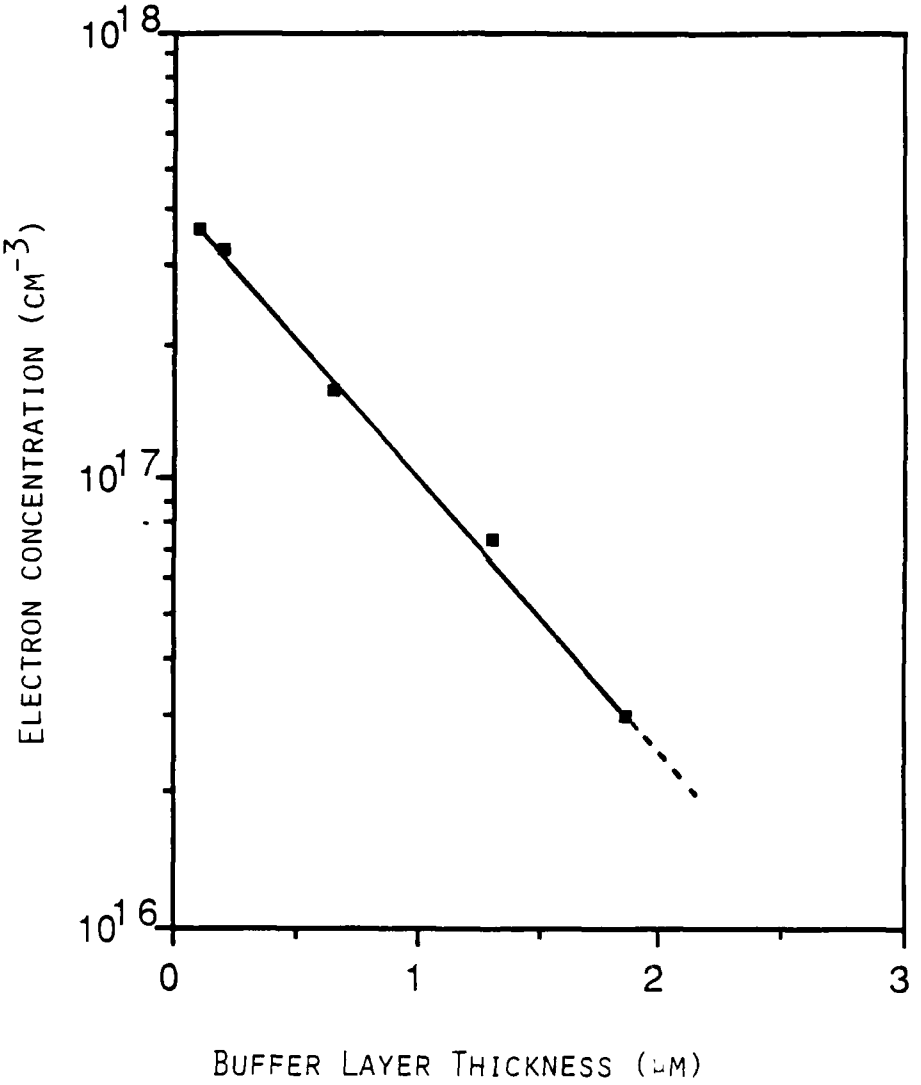
10^{18}
10^{17}
10^{16}
ELECTRON CONCENTRATION (CM^{-3})
0
1
2
3
BUFFER LAYER THICKNESS (μM)

FIG 4 b

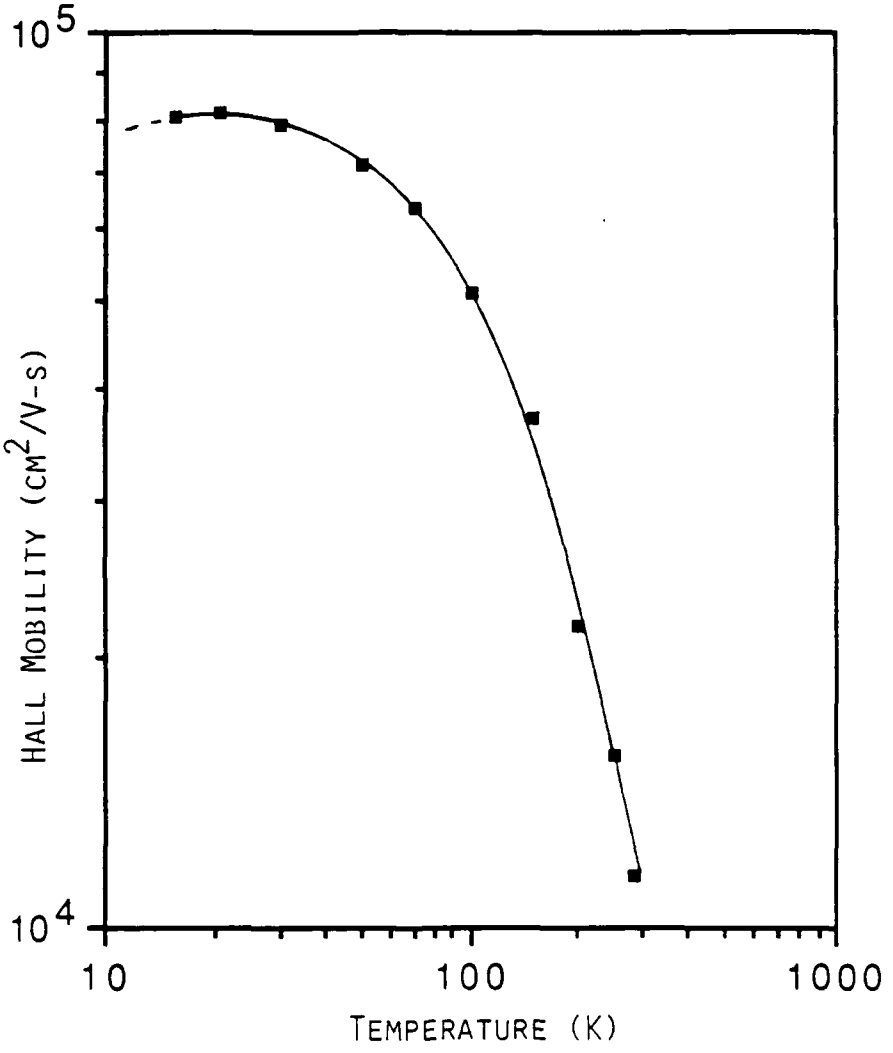

FIG 5a

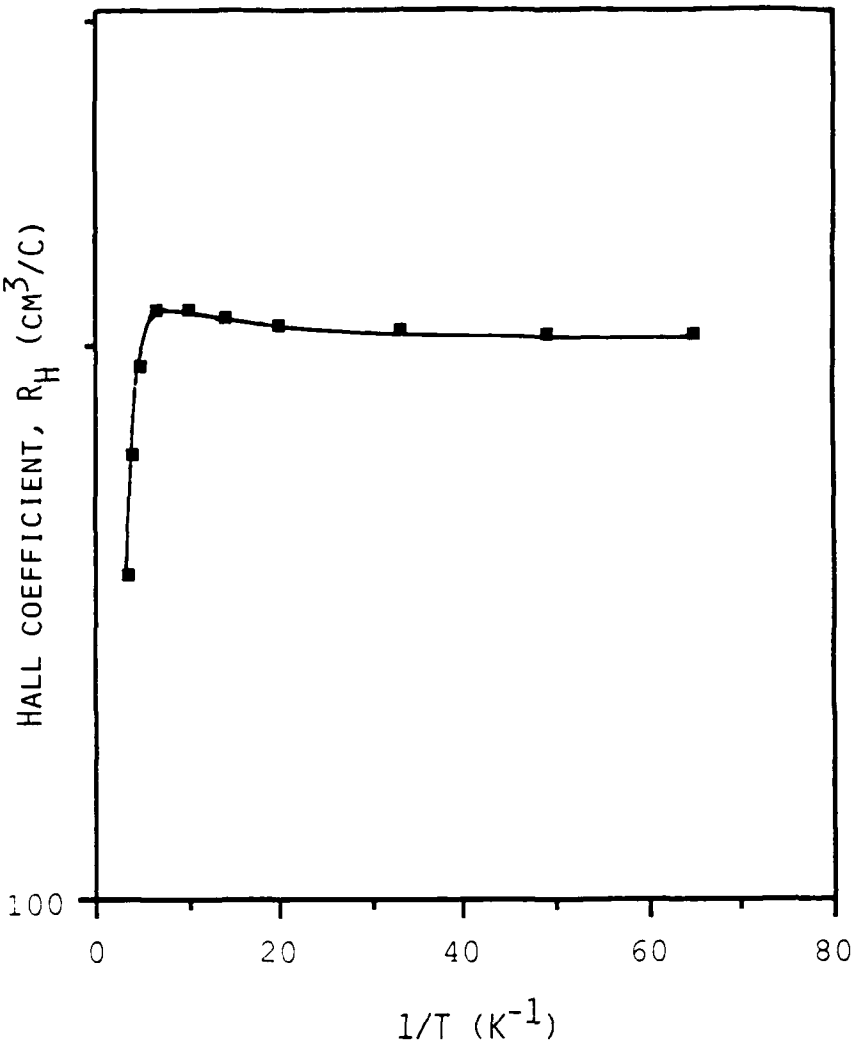

FIG 5 b

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Characteristics of OMVPE-grown CdTe and HgCdTe on GaAs

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Abstract

CdTe layers grown on GaAs have been characterized by photoluminescence measurements (PL), transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS). PL spectra of layers less than about 1.1 μm show a shift to lower energy of the exciton band, which we attribute to the compressive strain in CdTe along the CdTe-GaAs interface. Layers thicker than 1.1 μm gave PL indicative of high quality layers of bulk CdTe. TEM studies have shown that the lattice mismatch is accommodated by misfit dislocations at the interface and some by lattice strain. As the layer grows thicker this strain is relieved by dislocation lines in the first micron of the layer. SIMS measurements on these layers indicate negligible Ga diffusion, confirming our earlier findings. High quality mercury cadmium telluride (MCT) layers have been grown on these CdTe buffers, with properties similar to layers grown on bulk CdTe substrates. Double crystal X-ray rocking curves of the best MCT layer grown on GaAs substrates show a full width at half maximum (FWHM) of about 110 arc seconds. The best FWHM obtained on MCT layers grown on CdTe substrates was 125 arc secs.

Introduction

$Hg_{1-x}Cd_xTe$ (MCT) is an important intrinsic semiconductor material for far infrared detector applications, and epitaxial growth of this material has received considerable attention in the past few years. CdTe is a natural choice as a substrate material because of its excellent lattice match and chemical compatibility with the MCT system. However, lack of availability of high quality, large area substrates of this material have prompted many workers to consider alternate substrates, especially GaAs[1-3]. A large lattice mismatch (≈13.6%) is present between CdTe and GaAs. Nevertheless, growth of high quality CdTe layers on GaAs substrates was found to be possible by both molecular beam epitaxy[4,5] (MBE) and organometallic vapor phase epitaxy (OMVPE)[6-10]. In this paper, we will describe the results of photoluminescence (PL), transmission electron microscopy (TEM), and secondary ion mass spectrometry (SIMS) studies of CdTe layers on GaAs, and double crystal X-ray diffraction (DCD) results of MCT grown on CdTe/GaAs substrates.

Experimental

The epitaxial growth of CdTe and MCT was carried out in a horizontal, atmospheric pressure, reactor using dimethylcadmium (DMCd), diethyltelluride (DETe) and mercury. GaAs substrates with (100)2°→(110) orientation were cleaned in organic solvents and etched in Caro's etch (H_2SO_4:H_2O_2:H_2O = 5:1:1 by volume) for 10 minutes.

This was followed by an etch in a solution of ammonium hydroxide, hydrogen peroxide and water (10:1:1) for about 30 seconds. Most of the CdTe growth in this study was done at 350°C under DETe rich growth conditions. MCT layers were grown at 415°C on top of this CdTe buffer layer.

For the PL measurements the samples were excited with the 4880 Å line of an Ar^+-ion laser, and the luminescence was analyzed with a double pass monochromator and detected with photon counting electronics. The high sensitivity of this system enabled PL measurements to be made on thin (≈0.1 μm) epitaxial layers.

Results and discussion

Photoluminescence measurements

Because of the large lattice mismatch between CdTe and GaAs, the epilayer is expected to have a biaxial, compressive strain along the direction parallel to the growth interface. To study this strain, we have taken PL measurements on CdTe layers of various thickness d, ranging from 0.1 μm to 2.6 μm. The near band-edge recombination in the PL spectra is shown

in Fig. 1. The PL-spectra of the CdTe layers with d≥1.1 μm are typical of high quality layers. They consist of a stronger band arising from the bound exciton transitions at 1.592eV and free exciton transitions at 1.596eV respectively. These positions agree with those reported for bulk CdTe crystals. With decreasing d, the PL peak broadens and the position of the peak shifts to lower energy. These shifts are attributed to biaxial compressive strains in CdTe along the epi-substrate interface[11]. For a layer of 0.1 μm thick, the shift in the position of the peak is about 7.2 meV. From the PL study it is seen that we need at least 1.1 μm of CdTe as a buffer layer so that high quality MCT layers can be grown on GaAs.

Transmission electron microscopy

Cross sectional TEM of CdTe layers of various thickness have been taken to study the nature of dislocations at the interface. Figure 2 shows a lattice fringe image of the interface region and is representative of all the epilayers investigated. The fringes correspond to pairs of (111) planes in both the substrates and epilayer, projected along a [110] direction. The interface appears to be atomically sharp without the presence of any oxide or foreign layer. Misfit dislocations spaced about 31 Å apart are seen at the interface. This result is identical to that reported on CdTe layers grown by MBE[12]. The epilayer is not completely relaxed by this array of dislocations. As the layer thickness is increased, additional dislocations are created from surface sources and migrate towards the interface under the influence of the remaining strain. This is shown in Fig. 3, a TEM photograph of a 2.6 μm thick CdTe. These dislocations are probably responsible for the complete relaxation of the lattice mismatch not taken up by the misfit dislocations[12]. The top region, above 1.3 μm, has a low density of dislocations. The interface region, about 500 Å thick, has a high density of dislocations which remains constant for samples of different layer thickness.

Secondary mass ion spectrometry

An important question that arises when MCT is grown on a foreign substrate is the doping of the layer by the substrate. In this case, Ga is an n-type dopant in both CdTe and MCT and out diffusion of Ga from the GaAs substrate can be a potential problem. To investigate this possibility, we have performed SIMS studies of several CdTe layers grown on GaAs. These measurements were done using oxygen ion bombardment and positive secondary ion spectrometry by Charles Evans & Associates. Figure 4 shows the SIMS profile of a ≈2 μm thick CdTe grown at 350°C with a growth rate of ≈2 μm/hour. It is seen that, within about 1000 Å, the Ga concentration falls to below the background level and remains constant at this value. (The increase in the concentration at the surface is probably due to some SIMS artifacts.) Figure 5 shows the SIMS profile of a CdTe layer grown at 350°C and held at 415°C for 1 hour under DMCd overpressure. This is done in order to see the effect of keeping the above CdTe layer at a time and temperature associated with MCT growth. The interdiffusion distance is still very small, the Ga concentration falling to below 1×10^{15} within about 0.5 μm. Hence, we can conclude that the Ga diffusion into MCT layers can be ignored if the CdTe buffer layer is at least 0.5 μm thick.

We have grown (111) CdTe at 375°C on (100) GaAs substrates after a 5 minute deoxidation step at 580°C. The Ga diffusion profile on such a layer is shown in Fig. 6. Here also we see negligible Ga diffusion. When this sample is heat-treated at 415°C for 1 hour, however, significant Ga diffusion is observed. This is shown in Fig. 7. Whether this diffusion is due to the high temperature heat-treatment step before the growth or because of the growth of the CdTe at higher temperature (375°C vs 350°C) is not clear at the present time. One possibility is that the high temperature heat-treatment leaves a Ga rich surface which acts as a diffusion source during the 415°C anneal step.

MCT growth

MCT layers have been grown on these CdTe buffer layers. The growth temperature used was 415°C and the layers were all 4.6 μm thick. MCT layers with a nominal composition x of 0.2 were grown with buffer layers of various thickness ranging from 0.2 μm to 2.6 μm. It was found that the thickness of the buffer layer has a strong effect on the electron mobility in the MCT layers. The electron concentration for these layers, measured at 77K, fell monotonically for increasing buffer layer thickness; concurrently, the electron mobility rose from 10^4 to 2×10^5 cm^2/Vs[7]. This is because, as the CdTe layer thickness is decreased, more of the strain due to the large lattice mismatch is accommodated in the MCT layer. Both the PL studies and the TEM studies of the CdTe layers strongly indicate that this reduction in the electron concentration is due to the reduced strain in the MCT layers, and not due to a reduction in the amount of Ga-diffusion from the substrate.

DCD curves of MCT layers have been taken using InSb as the first crystal. Figure 8 shows a rocking curve of a 6 μm thick MCT layer grown on GaAs with a 2.6 μm buffer layer of CdTe. A full width at half maximum of 110 arc seconds is the lowest reported for MCT grown by OMCVD. This value was found to be uniform within 10 arc seconds over a 7 x 7 mm area. Layers grown on CdTe substrates had a FWHM of 125 arc secs, which indicates that 2-3 μm

thick CdTe buffer layer is enough to completely relieve the strain caused by the lattice mismatch.

Conclusion

CdTe layers have been grown on (100) GaAs by OMCVD and characterized by PL, TEM and SIMS measurements. PL spectra of layers less than 1.1 μm show a shift to lower energy of the exciton band, which we attribute to the compressive strain along the CdTe-GaAs interface. Layers thicker than 1.1 μm were found to be without any strain, as shown by PL measurements. TEM studies have shown that when the CdTe layer is thin, some of the lattice mismatch is accommodated by misfit dislocations and some by the lattice strain. As the layer grows thicker this strain is relieved by dislocations. This also agrees with the PL studies. SIMS measurements done on these layers shows negligible Ga diffusion even after prolonged heat-treatment at the growth temperature. High quality MCT layers can be grown on these buffer layers and their properties are similar to the layers grown on bulk CdTe substrates. The DCD rocking curve of the best MCT layer shows a FWHM of about 110 arc seconds.

Acknowledgement

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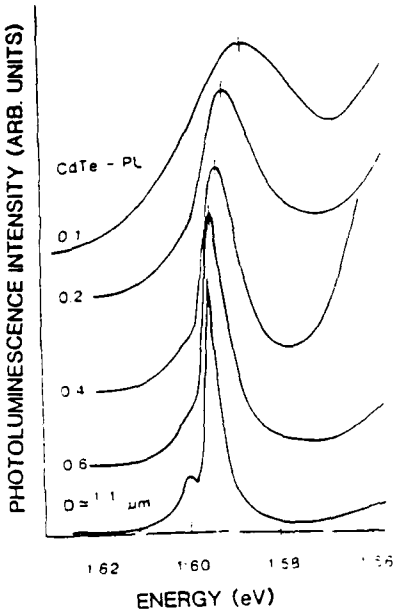

Figure 1. Photoluminescence spectra of CdTe layers for selected values of layer thickness d.

Figure 2. Lattice fringe image of the CdTe-GaAs interface using a systematic row of (110) relfections and transmitted beam in the (110) projection. The interface is delineated by array of misfit dislocations marked M.

Figure 3. Bright field image of the 2.2 μm epilayer showing the dislocation lines in the first 1 μm. Beyond the first 1 μm, the layer has low density of defects.

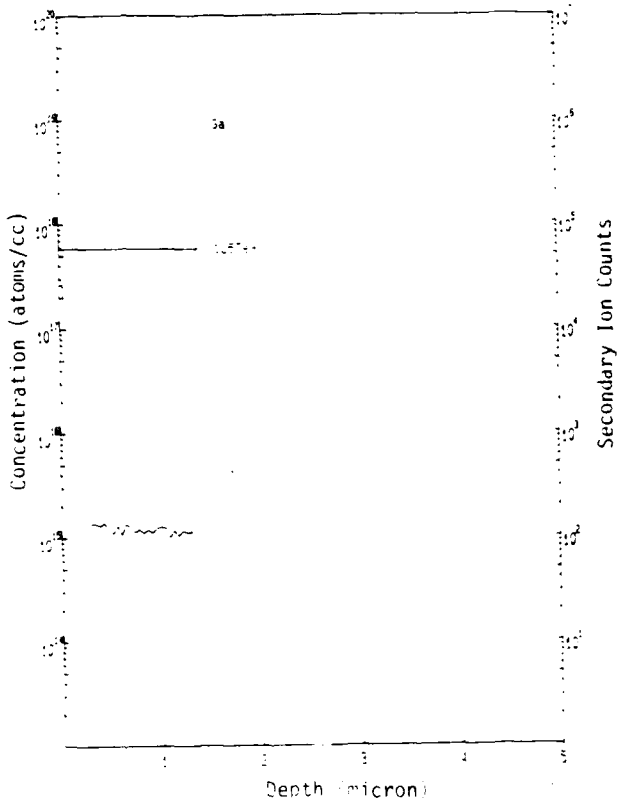

Figure 4. SIMS profile of a 2 μm thick CdTe layer, grown at 350°C, with a growth rate of 2 μm/hr.

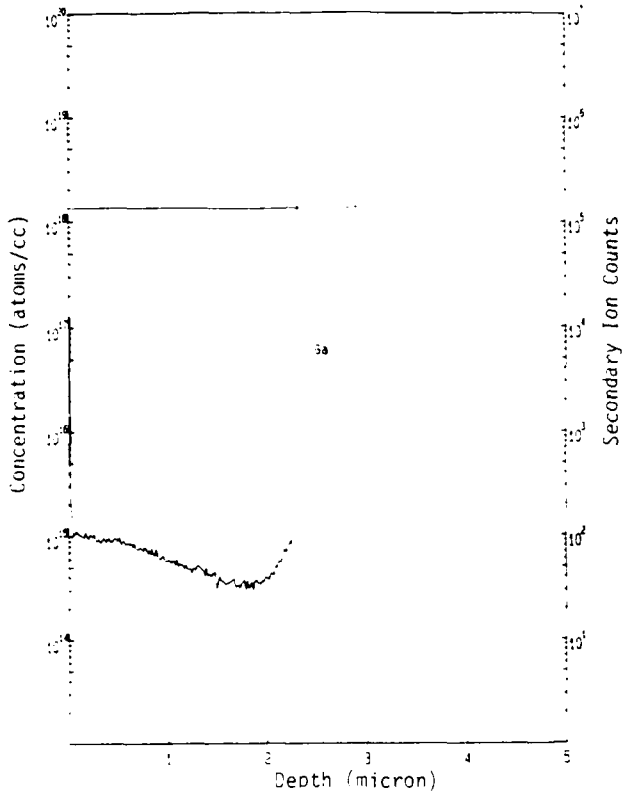

Figure 5. SIMS profile of a ~2 μm thick CdTe layer grown at 350°C, and annealed at 415°C for 1 hour.

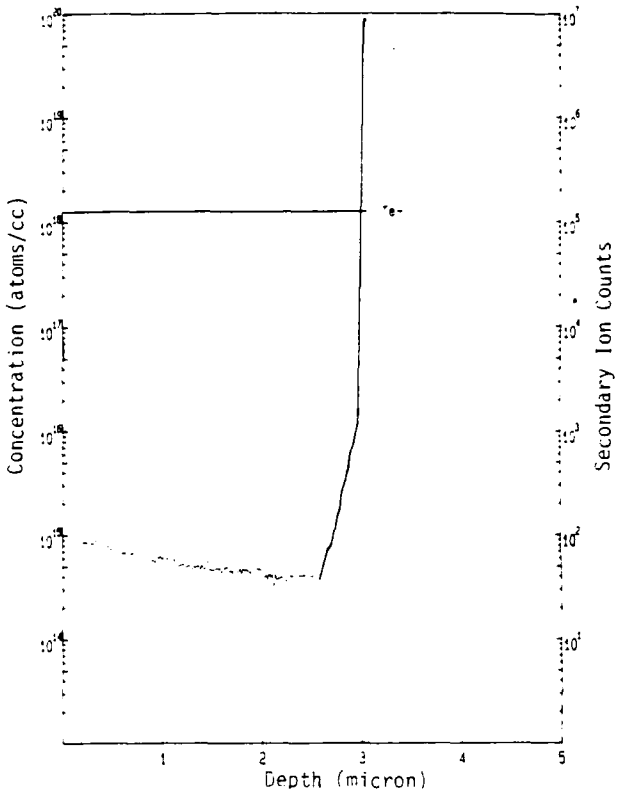

Figure 6. SIMS profile of a ~3 μm thick layer grown at 375°C with a 580°C deoxidation step.

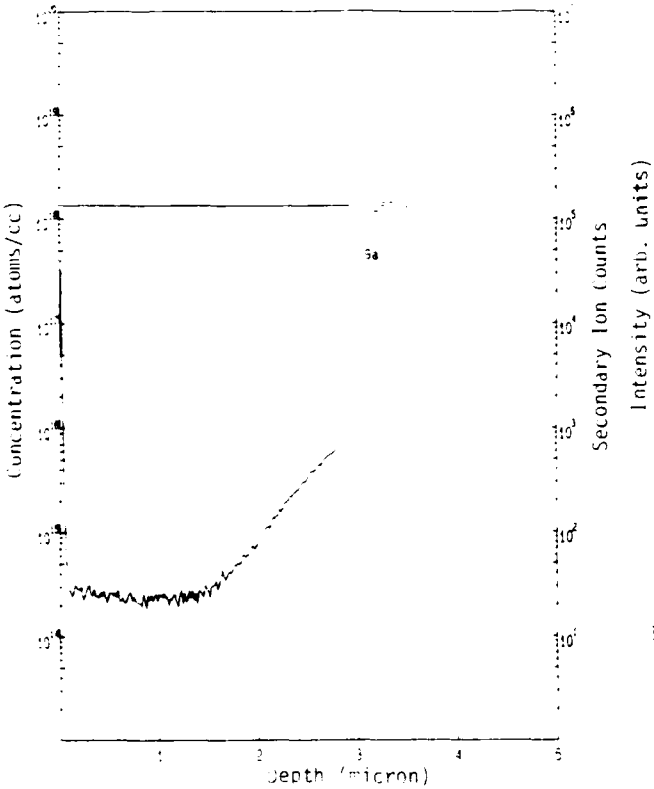

Figure 7. SIMS profile of the above layer after annealing step at 415°C for 1 hour.

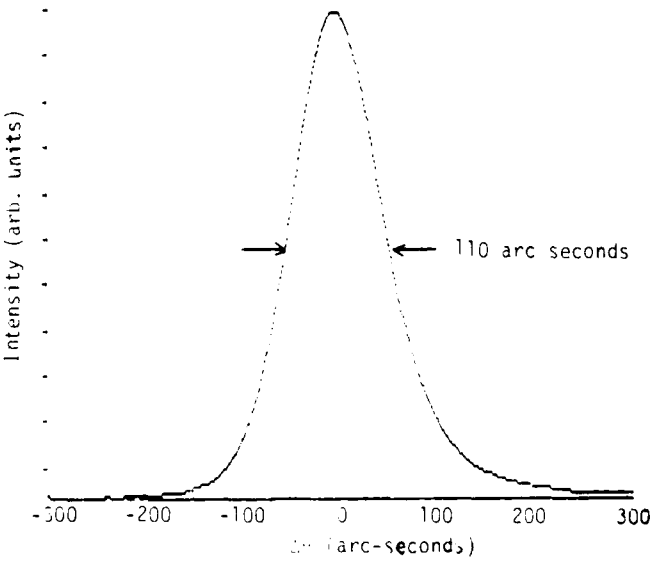

Figure 8. Double crystal X-ray rocking curve of 6 μm thick MCT layer grown on a 2.6 μm thick CdTe buffer layer. The nominal composition of the MCT layer, x = 0.2.

Organometallic epitaxy of HgCdTe on CdTeSe substrates with high compositional uniformity

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We report here on the growth of $Hg_{0.8}Cd_{0.2}Te$ on lattice-matched substrates of $CdTe_{0.96}Se_{0.04}$ by organometallic vapor phase epitaxy. Results are compared with those for comparable layers grown on CdTe substrates. It is shown that the use of lattice-matched substrates results in active layers of improved structural quality, as evidenced by the results of double-crystal x-ray diffraction measurements. A compositional uniformity of better than ± 0.005 (in the Cd composition) was obtained over 1 cm $\times$ 2 cm area substrates, corresponding to a standard deviation of 0.0024. The thickness uniformity was better than $\pm 0.7\,\mu$m for 12-μm-thick layers. These layers were deposited by the direct alloy growth, without the interdiffusion of separate layers of HgTe and CdTe. Both *n*- and *p*-type layers have been grown by suitable modification to the growth process. Mobility values in excess of 6×10^5 cm^2/V s were obtained in *n*-type material ($x = 0.2$), with an electron concentration below 1×10^{15} cm^{-3}. With *p*-type layers, mobility values of 400 cm^2/V s were obtained with a hole concentration of 1×10^{17} cm^{-3}.

The growth of $Hg_{1-x}Cd_xTe$ by organometallic vapor phase epitaxy (OMVPE) has previously been reported,[1-6] where elemental mercury and dimethylcadmium were used together with diethyltelluride as the tellurium source. The use of diisopropyltelluride[7] has enabled a reduction of the growth temperature to 370 °C, and newer tellurium sources[8,9] should allow growth of HgCdTe to 350 °C or lower. Thus, OMVPE has become the prime candidate among the currently available epitaxial growth techniques for this material, offering many features such as low temperature of growth and the potential for volume production.

CdTe substrates, or GaAs substrates with an intervening CdTe buffer layer, have been used for the growth of $Hg_{1-x}Cd_xTe$. In either case, the lattice mismatch between $Hg_{1-x}Cd_xTe$ with $x = 0.2$ and CdTe will generate dislocations at the interface which will glide into the epilayer. Alternate substrates, such as $Cd_{1-w}Zn_wTe$ ($w \simeq 0.04$) of $CdTe_{1-y}Se_y$ ($y \simeq 0.04$), have been proposed,[10,11] which are lattice matched to $Hg_{0.8}Cd_{0.2}Te$. The addition of either Se or Zn into CdTe also increases its hardness and reduces the dislocation density of bulk grown substrates, so that these are inherently better starting materials than CdTe. These substrates have been used for the growth of HgCdTe by liquid phase epitaxy, and a reduction in the interface dislocations by more than two orders of magnitude has been reported,[11] supporting the importance of close lattice matching.

CdTeSe and CdTeZn are both grown by the addition of small amounts of Se and Zn, respectively, into a CdTe melt. Here, the use of Se is advantageous since it has a distribution coefficient of about 0.97, compared to about 1.31 for Zn. As a result, compositional control of the substrate is maintained over larger boule lengths, so that CdTeSe is potentially a less expensive substrate material than CdTeZn. In this letter, we report for the first time on the OMVPE growth of $Hg_{0.8}Cd_{0.2}Te$ on $CdTe_{0.96}Se_{0.04}$ substrates, to which it is closely lattice matched.

HgCdTe layers have been grown by conventional OMVPE, in which growth is accomplished by simultaneous deposition of the relevant components Te, Cd, and Hg. A stationary, resistance heated susceptor was used in a vertical reactor configuration. Diisopropyltelluride and dimethylcadmium were the tellurium and cadmium sources, respectively, and elemental mercury was used as the Hg source. $CdTe_{0.96}Se_{0.04}$ substrates, obtained from II-VI Inc., Saxonburg, PA, were used for this work. These were (100), misoriented 2° → (110). All the growth runs were made at reduced pressure (380 Torr) and at a susceptor temperature of 390 °C. We estimate the actual substrate temperature to be ~20 °C lower. The growth rates were approximately 3.5 μm/h for all runs.

Fourier transform infrared (FTIR) transmission spectroscopy has been used to study the compositional uniformity across the wafer. This technique is nondestructive; moreover, its sensitivity is comparable to or better than that of alternative methods. The typical infrared transmission curves from five points on a 7.1-μm-thick, 1 cm $\times$ 1 cm area sample are shown in Fig. 1. The infrared beam size was 1 mm in diameter. We note that the transmission curve is relatively sharp for a composition of $x \simeq 0.2$. The sharp interface between the HgCdTe and the substrate is demonstrated by the well-defined interference fringes. Excellent thickness uniformity is evident from the overlapping interference fringes of the transmission curves from different areas of the substrate, which are indicated in the figure.

The interference fringes were used to determine the thickness of the epilayer, using $t = 1/(2n\Delta\omega)$, where $\Delta\omega$ is the fringe spacing near the 10–20 μm region and n is the refractive index of the epilayer. The refractive index is a function of composition and the wavelength, but was taken as 3.55 for material with $x \simeq 0.2$.[12] The band gap of the layer was determined by the energy at which the transmission corresponds to an absorption coefficient $\alpha = 500$ cm^{-1}. This

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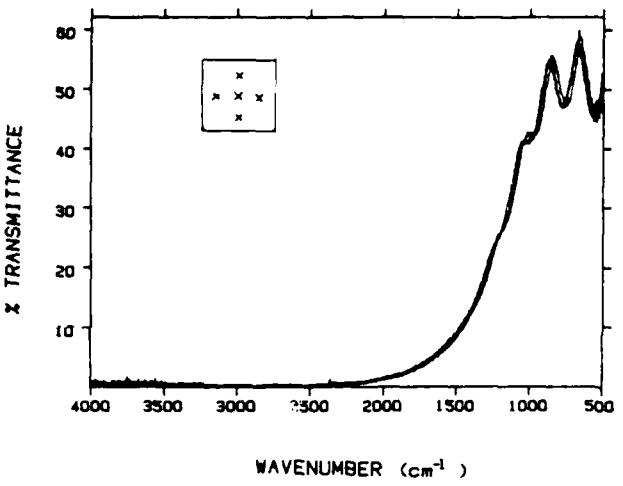

FIG. 1. Infrared transmission curves from five points on a 1 cm × 1 cm area $Hg_{0.81}Cd_{0.19}Te$ layer. The location of the points is marked in the figure. The infrared beam size was 1 mm in diameter.

point was calculated using the expression $T = T_{max}e^{-t}$, where T_{max} is the maximum transmission and t is the layer thickness. The composition of the layer was determined at each point from the relationship given in Ref. 13.

Table I shows the composition map of a HgCdTe layer grown on a 1 cm × 2 cm area CdTeSe substrate. The infrared beam size was 2 mm in diameter in this case, and the entire wafer was scanned using a computerized x-y translational stage, with a step size of 2.5 mm. One important feature to note is that layers have edge to edge compositional uniformity (Cd fraction) of better than ± 0.005 (standard deviation = 0.0024) over the whole area and better than ± 0.002 (standard deviation = 0.0014) over a 1 cm × 1 cm area. The thickness uniformity of the layer is also excellent, better than $\pm 0.7\,\mu$m for 12-μm-thick layers. Many layers have been grown with the above composition of $x \simeq 0.2$, and the uniformity was found to be reproducible from run to run.

TABLE I. Composition and thickness map of a HgCdTe layer grown on a 1 cm × 2 cm area CdTeSe substrate. The values in the parentheses are the layer thickness in microns.

Distance y_{mm}/x_{mm}	0	2.5	5	7.5
0	0.190	0.192	0.193	0.195
	(12.4)	(12.4)	(11.8)	(11.8)
2.5	0.189	0.192	0.193	0.194
	(12.6)	(12.6)	(12.0)	(12.2)
5	0.189	0.191	0.192	0.193
	(12.6)	(12.6)	(12.2)	(11.9)
7.5	0.190	0.191	0.192	0.192
	(12.6)	(12.4)	(12.2)	(12.0)
10.5	0.191	0.192	0.192	0.192
	(12.6)	(12.2)	(11.8)	(11.9)
12.5	0.194	0.194	0.194	0.193
	(11.8)	(11.8)	(11.8)	(11.9)
15	0.197	0.196	0.194	0.192
	(11.8)	(11.8)	(11.9)	(11.8)
17.5	0.199	0.198	0.192	0.189
	(11.2)	(11.6)	(12.2)	(12.3)

This is the first time such compositional uniformity has been demonstrated over this large area, using conventional alloy growth techniques by OMVPE. Layers of comparable uniformity have been grown[14,15] using an interdiffused multilayer process, where alternate layers of CdTe and HgTe are grown under optimized growth conditions for each binary compound, and homogenized at the growth temperature with an annealing step. However, this involves an interdiffusion process which requires a rather high temperature, and offsets the advantage of low-temperature growth. In addition, the crystallinity of interdiffused HgCdTe has been shown to be poorer than that of alloy grown HgCdTe, as determined by double-crystal x-ray diffraction.[16] This has been attributed to crystalline defects generated due to the lattice mismatch between HgTe and CdTe, and to incomplete interdiffusion. Thus, the conventional alloy growth technique is potentially more suitable for devices, if compositional uniformity is achieved as demonstrated here.

Double-crystal x-ray measurements have been made to determine the effect of lattice matching in improving the crystal quality. Figure 2 shows a map of x-ray full width at half-maximum (FWHM) values of 12-μm-thick HgCdTe layers grown simultaneously on CdTe and CdTeSe substrates. The composition of this layer was $x = 0.182 \pm 0.003$ over the whole area. Note that, even for a layer of this thickness, the effect of lattice mismatch is clearly evident from the results on CdTe substrates. The FWHM value of double-crystal rocking curves for layers grown on CdTeSe substrates is 47 ± 2 arcseconds, which is one of the lowest values reported for $HgCdTe_3$ epitaxial layers. The comparable values for the layer grown on CdTe are 151 ± 15 arcseconds.

The x-ray measurements were also made on the CdTeSe and CdTe substrate material. Here, CdTeSe substrates had FWHM values of ≃ 14 arcseconds and CdTe substrates gave values of about 32 arcsecond. Thus, in addition to CdTeSe being a better lattice match to HgCdTe, its crystal quality is superior to that of CdTe. However, we think the significant improvement in the quality of HgCdTe layers grown on CdTeSe substrate is primarily due to its better lattice match to the substrate.

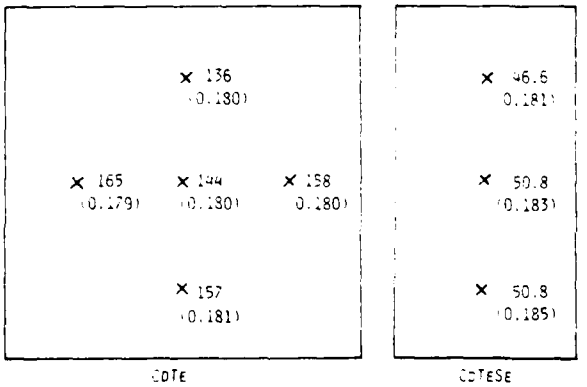

FIG. 2. Map of x-ray full width at half-maximum values (in arcseconds) for a 12-μm-thick HgCdTe layer grown simultaneously on 1 cm × 1 cm CdTe and 0.5 cm × 1 cm CdTeSe substrates. The values in the parentheses represent the Cd composition.

Immediately after growth, a 0.5-μm-thick cap of CdTe was grown as a protective coating. These samples showed classical *p*-type behavior. The hole carrier concentrations for these layers ranged from 5 to 10 $\times 10^{17}$ cm^{-3}, with hole mobilities in the 400–650 cm^2/V s range at 77 K. Some layers were grown without the CdTe cap and annealed, *in situ*, at 300 °C, for 1 h under a Hg overpressure. These layers converted to *n* type. The carrier concentration was below 1×10^{15} cm^{-3}, and mobility was in excess of 6×10^5 cm^{-2}/V s at 20 K, for layers with $x \simeq 0.2$. This illustrates that the electrical quality of this material is now suitable for large area photoconductive as well as photovoltaic applications.

In conclusion, we have shown that the use of CdTeSe substrates instead of CdTe gives HgCdTe layers with better crystal quality as determined by double-crystal x-ray diffraction data. The FWHM value for $Hg_{0.8}Cd_{0.2}Te$ grown on $CdTe_{0.96}Se_{0.04}$ is about 47 arcseconds, which is one of the lowest values reported for this material, and about three times smaller than that for layers grown simultaneously on CdTe substrates. Large area, highly uniform HgCdTe layers were grown using conventional OMVPE techniques. Layers grown in a vertical reactor without substrate rotation, had a Cd compositional uniformity of ± 0.005 (standard deviation = 0.0024) over a 1 cm $\times$ 2 cm area substrate. By employing a substrate rotation technique, we believe that we can improve the uniformity to better than ± 0.002 over this area. The layers are electrically of very high quality, with background carrier concentration of less than 1×10^{15} cm^{-3} for *n*-type material with $x \simeq 0.2$.

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HIGHLY UNIFORM, LARGE AREA HgCdTe LAYERS ON CdTe AND CdTeSe SUBSTRATES

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ABSTRACT

We report here on the growth of $Hg_{0.8}Cd_{0.2}Te$ on lattice matched substrates of $CdTe_{0.96}Se_{0.04}$, by organometallic vapor phase epitaxy. Layer properties are compared with those for comparable layers grown on CdTe substrates. It is shown that the use of lattice matched substrates results in active layers of improved structural quality, as evidenced by the results of double crystal x-ray diffraction measurements.

A compositional uniformity of better than ± 0.005 (in the Cd composition) was obtained over 1 cm $\times$ 2 cm area substrates, and the thickness uniformity was better than ± 0.7 μm for 12 μm thick layers. These layers were deposited by the direct reaction of mercury, dimethylcadmium, and diisopropyltelluride, without the interdiffusion of separate layers of HgTe and CdTe.

Both n and p-type layers have been grown, by suitable adjustment of the growth process. Mobility values in excess of 6×10^4 cm^2/V-sec were obtained in n-type material ($x = 0.23$), with an electron concentration below 1 x 10^{15} cm^{-3}. With p-type layers, mobility values of 680 cm^2/V- sec were obtained, with a hole concentration of 5×10^{16} cm^{-3}.

INTRODUCTION

The growth of $Hg_{1-x}Cd_xTe$ by organometallic vapor phase epitaxy (OMVPE) has previously been reported [1-7], where elemental mercury and dimethylcadmium were used together with diethyltelluride or diisopropyltelluride as the tellurium source. The use of diisopropyltelluride and other tellurium sources [8, 9] allows the growth temperature of HgCdTe to be reduced to 300°C or lower. Thus, OMVPE has become the prime candidate among the currently available epitaxial growth techniques for this semiconductor, offering many important features such as low growth temperature and the potential for volume production.

CdTe substrates, or GaAs substrates with an intervening CdTe buffer layer, are commonly used for the growth of $Hg_{1-x}Cd_xTe$. In either case, the lattice mismatch between $Hg_{1-x}Cd_xTe$ with $x = 0.2$ and CdTe will generate dislocations at the interface which will glide into the epilayer. Alternate substrates, such as $Cd_{1-w}Zn_wTe$ ($w \simeq 0.04$) or $CdTe_{1-y}Se_y$ ($y \simeq 0.04$), have been proposed [10, 11], which are lattice matched to $Hg_{0.8}Cd_{0.2}Te$. The addition of either Se or Zn into CdTe also increases its hardness and reduces the dislocation density of bulk grown substrates, so that these are inherently better starting materials than CdTe. These substrates have been used for the growth of HgCdTe by liquid phase epitaxy, and a reduction in the interface dislocations by more than two orders of magnitude has been reported [11], supporting the importance of close lattice matching.

CdTeSe and CdTeZn are both grown by the addition of small amounts of Se and

Zn respectively into a CdTe melt. Here, the use of Se is advantageous since it has a distribution coefficient of about 0.97, compared to about 1.31 for Zn. This allows compositional control of the substrate to be held over larger boule lengths, so that CdTeSe is potentially a less expensive substrate material than CdTeZn. In this paper, we describe the OMVPE growth of $Hg_{0.8}Cd_{0.2}Te$ on $CdTe_{0.96}Se_{0.04}$ substrates, to which it is closely lattice matched. Properties of these layers are compared to those grown on CdTe substrates.

EXPERIMENTAL

HgCdTe layers have been grown by conventional OMVPE, in which growth is accomplished by simultaneous deposition of the relevant components Te, Cd and Hg. A stationary, resistance heated susceptor, was used in a vertical reactor configuration. Diisopropyltelluride and dimethylcadmium were the tellurium and cadmium sources respectively, and elemental mercury was used as the Hg source. CdTe and $CdTe_{0.96}Se_{0.04}$ substrates, obtained from II-VI Inc., Saxonburg, PA, were used for this work. These were (100), misoriented $2° \rightarrow (110)$. All the growth runs were made at reduced pressure (380 torr) and at a susceptor temperature of 390°C. We estimate a substrate temperature of 360-370°C for our particular gas flow conditions. The growth rates were approximately 3.5 μm/hr for all runs.

The thickness and the composition of the layers was determined using Fourier transform infrared (FTIR) transmission spectroscopy. The thickness was calculated using the expression $t = 1/(2\ n\ \Delta w)$ where Δw is the fringe spacing near the 10-20 μm re-

gion, and n is the refractive index of the epilayer. The refractive index is a function of composition and the wavelength, but was taken as 3.55 for material with $x \simeq 0.2$ [12]. The bandgap of the layer was determined by the energy at which the transmission corresponds to an absorption coefficient $\alpha = 500\ \text{cm}^{-1}$. This point was calculated using the expression $T=T_{max}\ e^{-t}$, where T_{max} is the maximum transmission and t is the layer thickness. The composition x of the layer was determined at each point from the relationship between x and the bandgap given in [13].

X-ray double crystal rocking (DCR) curves were taken using Cu-K_α radiation, with InSb as the first crystal. Hall and resistivity measurements were made over a temperature range of 14 to 300K, at a magnetic field strength of 2.1KG. Gold was evaporated to make contact to p-type layers, and indium was used for electrical measurements of n-type layers.

RESULTS:

Figure 1 shows a photograph of a 1 cm $\times$ 2 cm area HgCdTe layer grown on a CdTeSe substrate. The layer is generally specular, but shows a regular terraced structure aligned along one of the (110) direction when viewed under high magnification. A typical surface morphology of a $Hg_{0.8}Cd_{0.2}Te$ layer on a CdTeSe substrate is shown in Fig. 2. Both CdTe and CdTeSe substrates resulted in layers with similar surface morphology.

Figure 3 shows the infrared transmission curve from five points on a 7.1 μm thick, 1 cm $\times$ 1 cm area sample. The infrared beam size was 1 mm in diameter. The transmis-

sion curve is relatively sharp for a composition of $x \approx 0.2$. The sharp interface between the HgCdTe and the substrate is demonstrated by the well defined interference fringes. Excellent thickness uniformity is evident from the overlapping interference fringes of the transmission curves from different areas of the substrate, which are indicated in the figure.

Figure 4 shows a map of 25% transmission cutoff points (λ_{25}) for a layer of 1 cm $\times$ 1 cm area. The entire wafer was scanned using a computerized x-y translation stage with a step size of 1 mm. The λ_{25} value over most of the area is within ± 0.15 micron, which corresponds to a compositional uniformity of better than ± 0.002 over this area. On a 1 cm $\times$ 2 cm area substrate, the composition x was within ± 0.005 over the whole area. The thickness uniformity of the layer is also excellent, better than ± 0.7 μm for 12 μm thick layers. Many layers have been grown with the above composition of $x \simeq 0.2$, and the uniformity was found to be reproducible from run to run.

This is the first time such compositional uniformity has been demonstrated over this large area, using conventional alloy growth techniques by OMVPE. Layers of comparable uniformity have been grown [14, 15] using an interdiffused multilayer process, where alternate layers of CdTe and HgTe are grown under optimized growth conditions for each binary compound, and homogenized at the growth temperature with an annealing step. However, this involves an interdiffusion process which requires a rather high temperature, and offsets the advantage of low temperature growth. In addition, the crystallinity of interdiffused HgCdTe layers has been shown to be poorer than that of alloy grown HgCdTe, as determined by double crystal x-ray diffraction [16]. This has been at-

tributed to crystalline defects generated due to the lattice mismatch between HgTe and CdTe, and to incomplete interdiffusion. Thus, the conventional alloy growth technique is potentially more suitable for devices, if compositional uniformity can be achieved as demonstrated here.

Double crystal x-ray measurements have been made to determine the effect of lattice matching in improving the crystal quality. Figure 5 shows a map of x- ray full width at half maximum values (FWHM) of 12 μm thick HgCdTe layers grown simultaneously on CdTe and CdTeSe substrates. The composition of these layers was $x = 0.182 \pm 0.003$ over the whole area. Note that, even for a layer of this thickness, the effect of lattice mismatch is clearly evident from the results on CdTe substrates. The FWHM value of double crystal rocking curves for layers grown on CdTeSe substrates are 47 $\pm$2 arc seconds, which is one of the lowest values reported for HgCdTe epitaxial layers. The comparable values for the layer grown on CdTe are 151 $\pm$15 arc seconds.

The x-ray measurements were also made on the CdTeSe and CdTe substrate material. Here, CdTeSe substrates had FWHM values of $\approx$14 arc seconds and CdTe substrates gave values of about 32 arc seconds. Thus, in addition to CdTeSe being a better lattice match to HgCdTe, its crystal quality is superior to that of CdTe. However, we propose that the significant improvement in the quality of HgCdTe layers grown on CdTeSe substrate is primarily due to its better lattice match to the substrate.

After growth, layers were annealed for one hour at 300° in a Hg overpressure. These layers were n-type. The carrier concentration below 1×10^{15} cm^{-3}, and mobility values in excess of 6×10^4 cm^2/V-sec at 20K, were obtained for layers with $x = 0.23$. Typical

mobility and Hall coefficient for a layer is shown as a function of temperature in Figs. 6 and 7. The mobility value does not fall off as temperature is decreased below ~40K. This indicates that the samples are not heavily compensated.

p-type layers have been grown, by capping the HgCdTe with a 0.5 μm thick CdTe. Classical p-type Hall curves are obtained for all capped layers. The p-type carrier concentration at 77K was in the range 5×10^{16} to 1×10^{17} cm^{-3} and Hall mobility in the range 400-700 cm^2/V- sec. Results for two representative samples are plotted in Figs. 8 and 9. At the growth temperature of 390° C, we expect as grown layers to be p- type due to the presence of Hg vacancies. These results indicate that the residual donor concentration in these layers is below 1×10^{15} cm^{-3}, and the electrical quality of this material is now suitable for large area photoconductive as well as photovoltaic applications.

CONCLUSION

We have shown that the use of CdTeSe substrates instead of CdTe gives HgCdTe layers with improved crystal quality as determined by double crystal x-ray diffraction data. The FWHM value for $Hg_{0.8}Cd_{0.2}Te$ grown on $CdTe_{0.96}Se_{0.04}$ is about 47 arc seconds, which is one of the lowest values reported for this material, and about three times smaller than that for layers grown simultaneously on CdTe substrates.

Large area, highly uniform HgCdTe layers were grown using conventional OMVPE techniques. Layers were grown in a vertical reactor without substrate rotation, and had a Cd composition uniformity of ± 0.005 over a 1 cm $\times$ 2 cm area substrate. By employing a substrate rotation technique, we believe that we can improve the uniformity to

better than ± 0.002 over this area. The layers are electrically of very high quality, with background carrier concentration of less than 1×10^{15} cm^{-3} for n-type material with $x \simeq 0.2$.

ACKNOWLEDGEMENT

The authors would like to thank J. Barthel for technical assistance on this program and P. Magilligan for manuscript preparation. This work was sponsored by the Defense Advanced Research Projects Agency (Contract Number N-00014-85- K-0151), administered through the Office of Naval Research, Arlington, Virginia. This support is greatly appreciated.

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FIGURES

Figure 1. Photograph of 1 cm × 2 cm area HgCdTe on $CdTe_{0.96}Se_{0.04}$ substrate.

Figure 2. Morphology of $Hg_{0.77}Cd_{0.23}Te$ layer grown on $CdTe_{0.96}Se_{0.04}$ substrate. The layer thickness ≈6.8 μm.

Figure 3. Infrared transmission curves from five points on a 1 cm × 1 cm area $Hg_{0.81}Cd_{0.19}Te$ layer. The location of the points are marked in the figure. The infrared beam size was 1 mm in diameter.

Figure 4. Composition uniformity map showing the variation of absorption cut-off (25% transmission point λ_{25}) for 1 mm diameter sampling area, over ~1 cm^2 area slice.

Figure 5. A map of x-ray full width at half maximum values (in arc- seconds) for a 12 μm thick HgCdTe layer grown simultaneously on 1 cm × 1 cm CdTe and 0.5 cm × 1 cm CdTeSe substrates. The values in the parentheses represent the Cd composition.

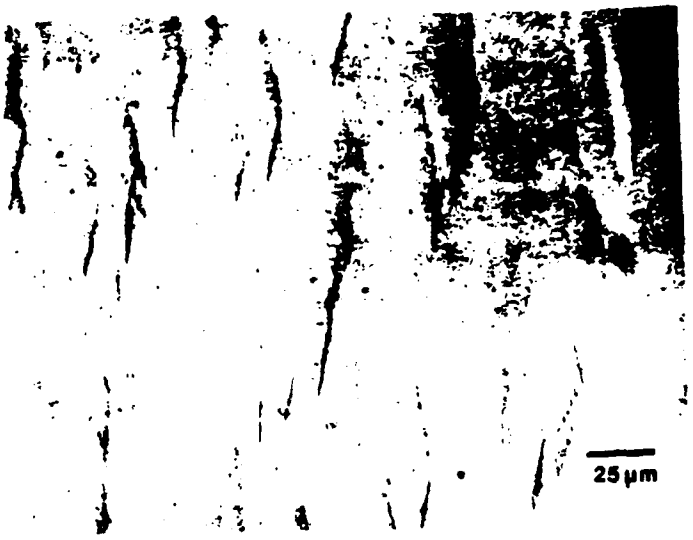
Figure 6. Hall mobility as a function of temperature for an n-type sample. Layer thickness 6.1 μm.

Figure 7. Hall coefficient as a function of temperature for the sample of Fig. 6.

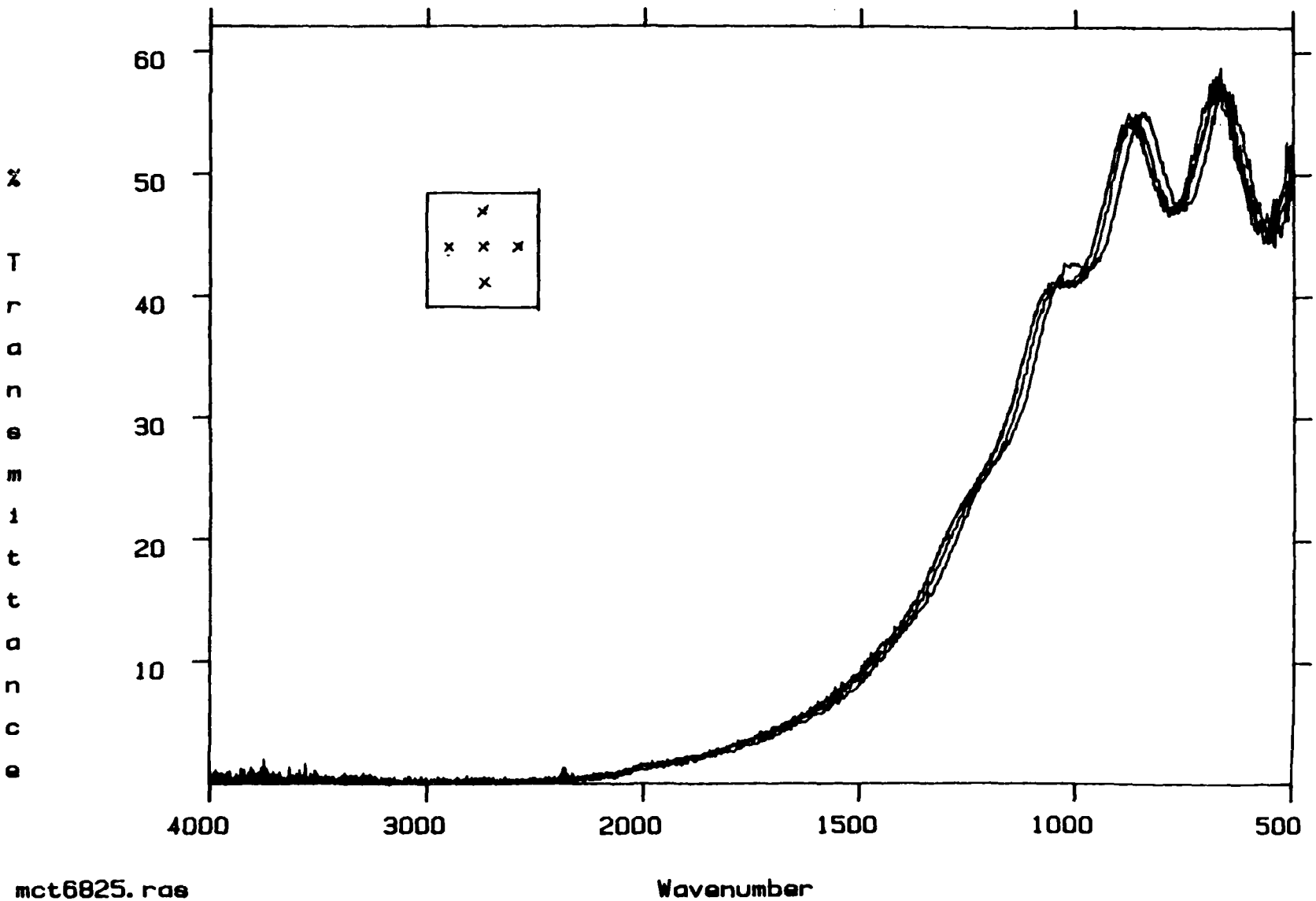
Figure 8. Hall mobility as a function of temperature for two p-type samples. (a) $x = 0.2$, thickness = 14μm, (b) $x = 0.26$, thickness = 10μm.

Figure 9. Variation of Hall coefficient as a function of temperature for the p-type layers of Fig. 8.

Shat et al
Fig 1



Bhat et al
Fig 2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8.47	8.23	8.18	8.18	8.18	8.18	8.18	8.10	8.28
8.44	8.25	8.25	8.23	8.23	8.23	8.28	8.28	8.36
8.28	8.28	8.31	8.25	8.31	8.31	8.31	8.31	8.41
8.38	8.23	8.23	8.25	8.33	8.36	8.36	8.33	8.58
8.33	8.18	8.23	8.28	8.36	8.38	8.38	8.31	8.61
8.23	8.10	8.23	8.25	8.31	8.31	8.31	8.31	8.52
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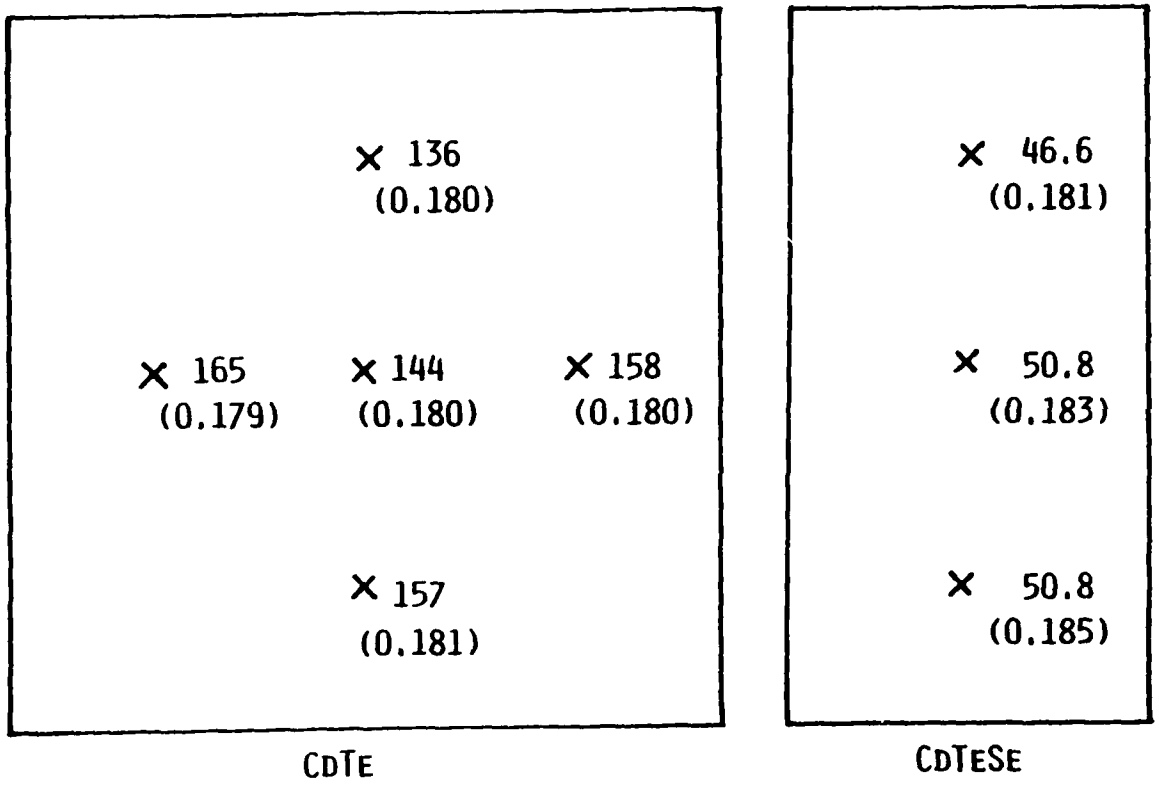
TCP FIG 4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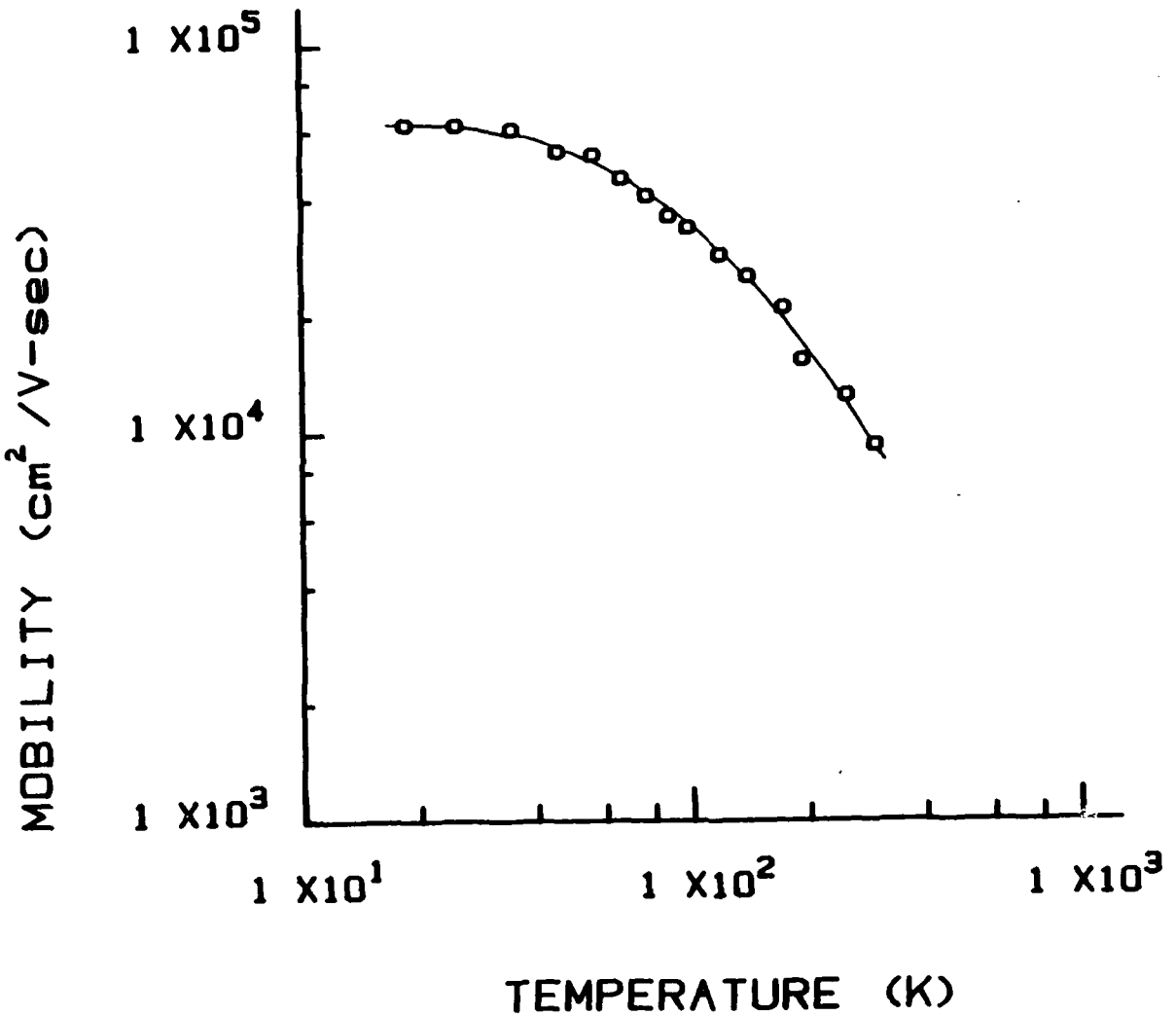
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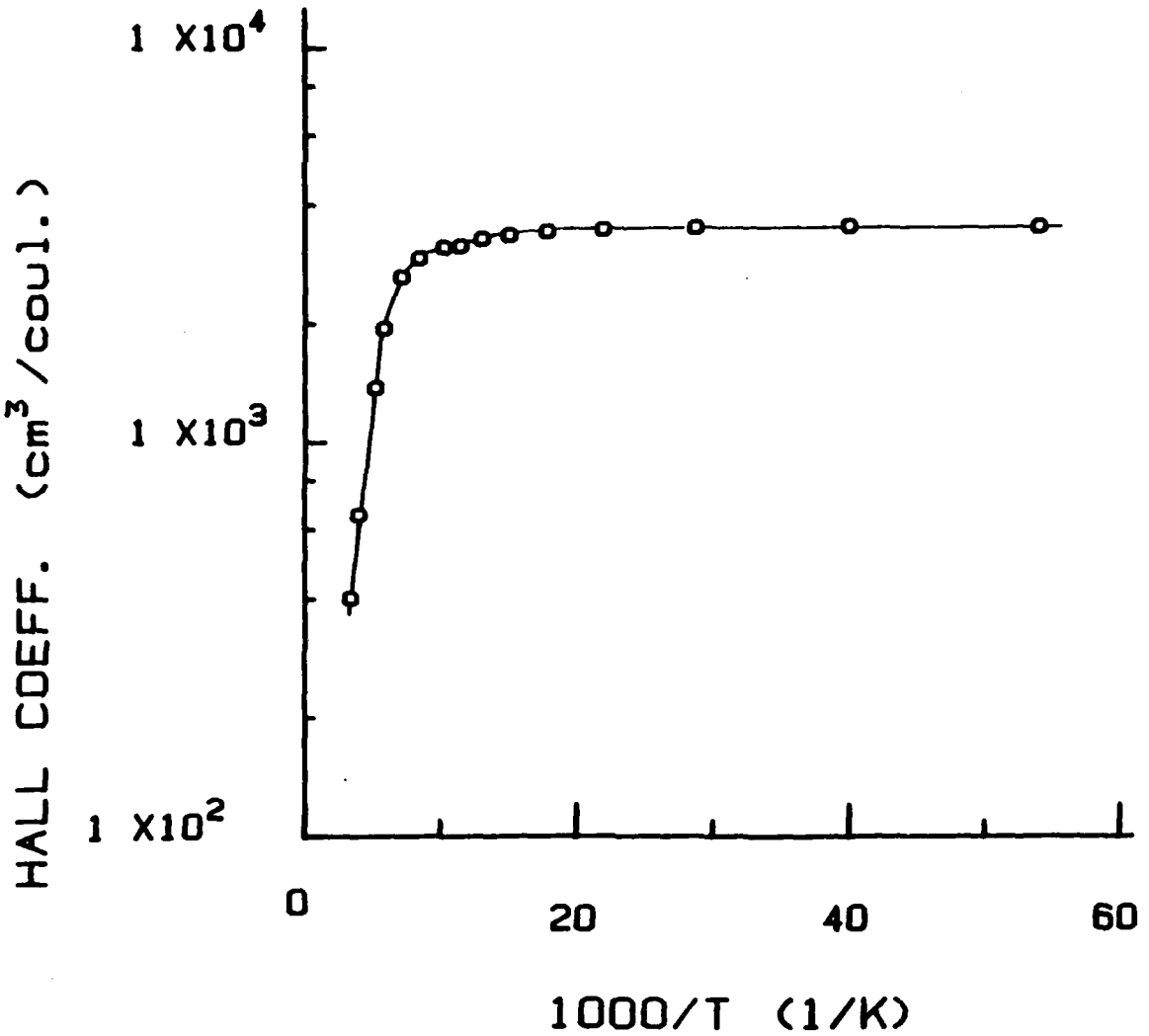
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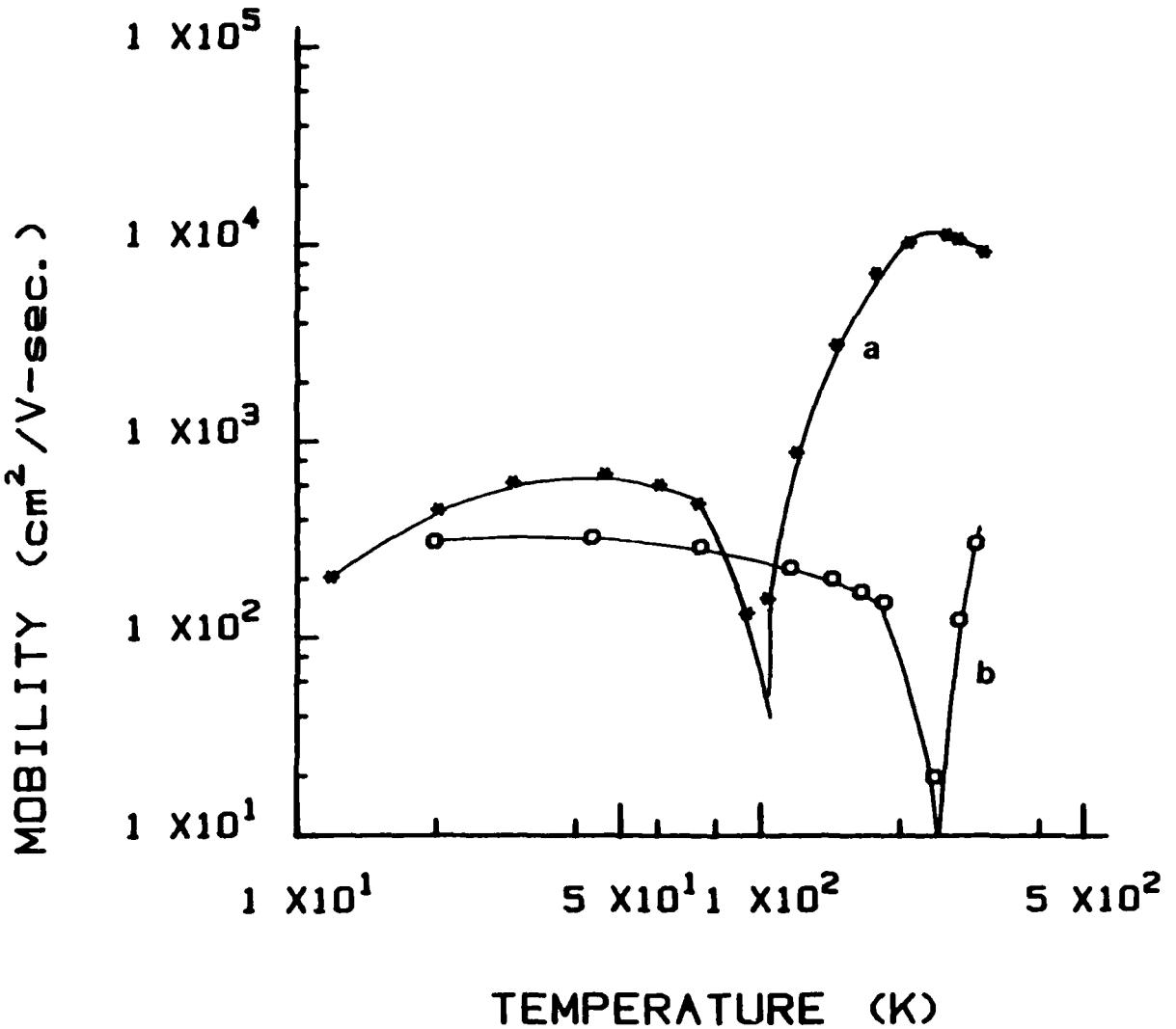
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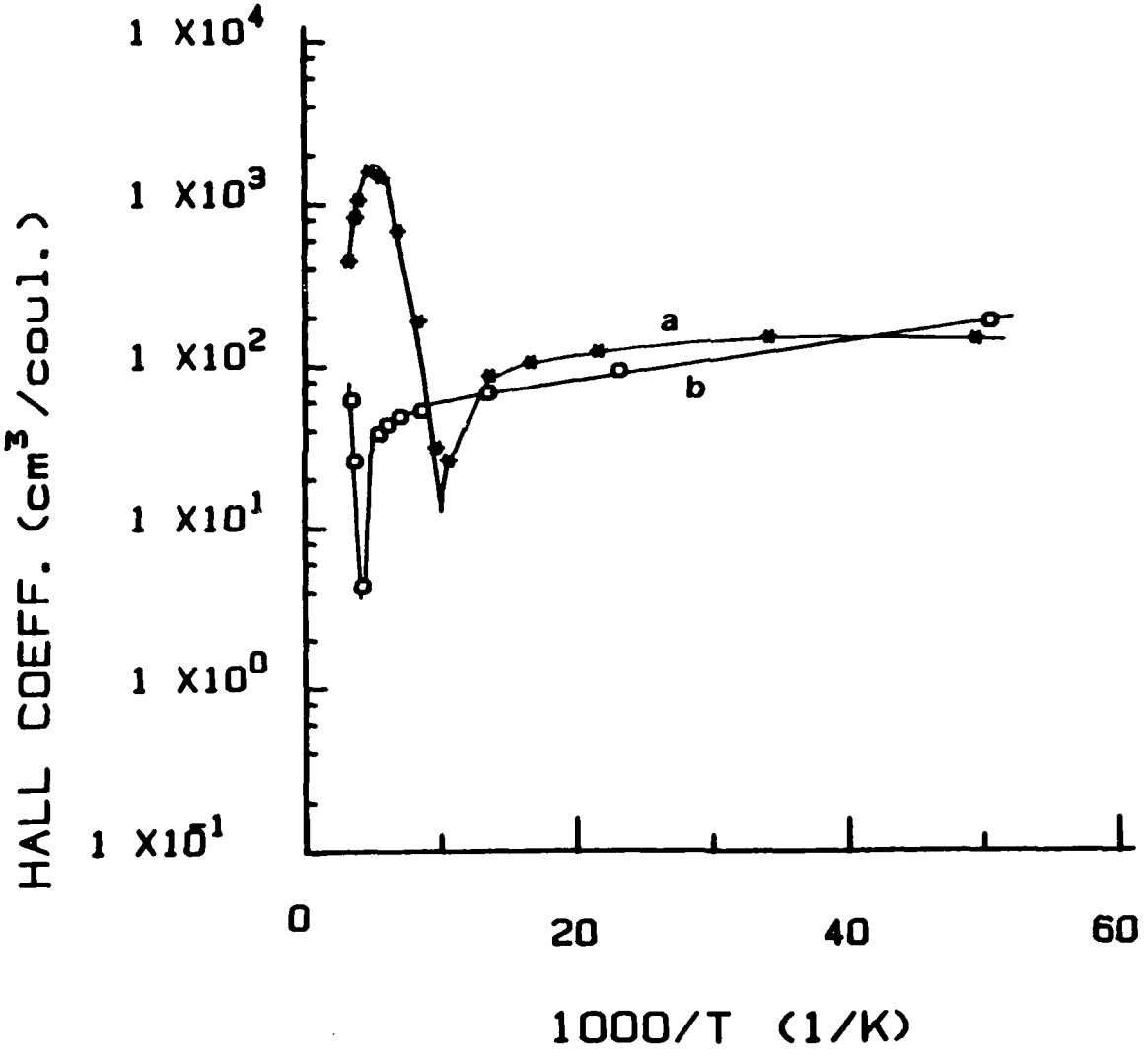
5 X10^2
TEMPERATURE (K)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20
40
60
1000/T (1/K)

THE ORGANOMETALLIC EPITAXY OF HgCdTe FOR INFRARED DETECTOR APPLICATIONS

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ABSTRACT

This paper reviews the requirements for mercury cadmium telluride material which is suitable for far infrared detectors. This is followed by substrate and reactor considerations, leading to its direct alloy growth by organometallic vapor phase epitaxy.

It is shown that HgCdTe can now be grown with electrical properties and areal compositional uniformity that are suitable for focal plane arrays, operating in the 10.6 μm range.

Technical

The epitaxial grown of $Hg_{1-x}Cd_xTe$ (MCT) has received considerable attention during the past several years, because it potentially can yield active layers of better electrical quality than those grown by bulk methods. Several methods have been reported for the growth of these layers; of these, organometallic vapor phase epitaxy (OMVPE) is a very promising candidate [1-8] for the eventual commercialization of this material.

The driving force behind the growth of MCT is that it is uniquely suited for focal plane array detectors, operating in the 10.6 μm range. Here, the main requirements are large area (1 cm $\times$ 1 cm or larger) with a compositional uniformity of better than $\pm$0.005 for x (Cd-fraction), and an x value around 0.2. Layers of 10-15 μm thickness are required for this application. Finally, since MCT is a semiconductor material in which defects are electronically active, layers with a high degree of crystalline perfection are essential for efficient detectors.

Substrates:

$Hg_{0.8}Cd_{0.2}Te$ layers are conventionally grown on bulk CdTe, to which they are lattice matched to within 0.3%. However, the lack of availability of high quality, large area substrates of this material have prompted many workers to consider alternative materials. Of these, InSb, which is closely lattice matched to CdTe, has been investigated by many workers. A disadvantage of using InSb as a substrate material is that it is optically opaque at wavelengths below 5 μm, so that it is unsuitable for many backside illuminated photodetector applications.

Other substrate materials [9, 10] are $Cd_wZn_{1-w}Te$ and $CdTe_{1-y}Se_y$. Both of these can be exactly matched to $Hg_{0.8}Cd_{0.2}Te$, provided that $w \simeq 0.04$ and $y \simeq 0.04$. With these materials, the addition of either Se or Zn into CdTe also increases their hardness and reduces the dislocation density of bulk grown substrates, so that these are inherently better starting materials than CdTe. These lattice matched substrates have been used for the growth of MCT by liquid phase epitaxy, and a reduction in the interface dislocations by more than two orders of magnitude has been reported, supporting the importance of close lattice matching. Both of these substrate materials have the advantage over InSb in that they are optically transparent in the far infrared.

CdTeSe and CdTeZn are both grown by the addition of small amounts of Se and Zn respectively into a CdTe melt. Here, the use of Se is advantageous since it has

a distribution coefficient of about 0.97, compared to about 1.31 for Zn. This allows compositional control of the substrate to be held over larger boule lengths, so that CdTeSe is potentially a less expensive substrate material than CdTeZn.

Recently, attention has focused on the use of GaAs as a substrate material, because of its excellent crystalline quality and low cost, as compared to all of the previous substrates. It is also transparent to the infrared range of wavelengths. Moreover, its use opens up the possibility of integrating GaAs circuits with sensor devices of MCT, in monolithic structures.

The lattice mismatch between MCT and GaAs is about 14% at room temperature. Consequently, it is necessary to grow a buffer layer of CdTe of sufficient thickness so as to accommodate the misfit-induced strain. This layer can be grown, together with the MCT layer, in a continuous process [12]. We have investigated strain in this CdTe layer by means of photoluminescence (PL) measurements of layers of varying thickness, grown on GaAs [11]. An argon laser was used to probe the upper regions of the CdTe layer, since its penetration depth is around 0.1 μm. CdTe layers, 0.1 μm-2.5 μm in thickness, were used for these experiments.

The measured PL spectra from the CdTe layers, as a function of the CdTe layer thickness D, are shown in Fig. 1. The PL-spectra of the CdTe layers with $D \geq 1.1\mu$m are typical of high quality layers. The near band edge spectrum consists of a stronger band arising from bound exciton transitions and a weaker structure peaking at higher energies and corresponding to recombinations involving free excitons. The positions of the bound and free excitons, $\approx$1.592 and 1.596 eV respectively, are the same as those reported for bulk crystals within experimental uncertainty. With decreasing D, a red shift and broadening of the CdTe PL-peaks take place. This can be attributed to biaxial compressive strains because of a shrinkage of the CdTe lattice. Figure 1 also shows that this shrinkage, and hence the associated strain in the upper layers of the CdTe, is negligible for buffer layers with thickness $\geq 1.1\mu$m.

Transmission electron microscope studies also show [13] a dramatic fall off in the dislocation density for layers thicker than this value. We conclude, therefore, that this represents the minimum buffer layer thickness for growth of high quality MCT layers. In our own work with the growth of MCT on GaAs, we have used 1.5-2.6 μm thick buffer layers of CdTe. This has resulted in MCT layers with the same mobility as we have achieved for layers grown on CdTe substrates. The effect of increasing buffer thickness is shown [14] in Fig. 2 for layers of MCT with $x \simeq 0.2$. Quantitative secondary ion mass measurements (C.A. Evans Associates) have shown that the out-diffusion of gallium from the substrate, and into the buffer, is under 0.25 μm. Thus, its effects can be completely ignored.

Growth Considerations:

Epitaxial growth of MCT on CdTe is conventionally carried out in a "warm" wall reactor system, at around one atmosphere, with palladium purified hydrogen as the carrier gas. Dimethylcadmium (DMCd) is used as the cadmium source. Typically, this liquid is held in a temperature controlled bubbler at 15°C, and its vapor delivered by passing hydrogen gas through the bubbler. Temperature control of the bubbler is critical, since the composition of the layer is a strong function of the partial pressure of the cadmium species. Diethyltellurium (DETe), conventionally used as the tellurium source, is introduced into the reactor in the same manner.

Elemental mercury is used as the third component for MCT growth. This requires a heated chamber to establish the necessary vapor pressure in the reactor. Accurate control

of the Hg-pressure is not as important as that for the Cd and Te sources. However, the necessity of a heated source requires the use of heated lines, unless the source is located in the reaction chamber.

The consumption of Hg in an OMVPE system is about 10-30 times less than for molecular beam epitaxial growth, because of differences in reactor operating pressures. Nonetheless, it is sufficiently large to preclude the use of organometallic sources such as dimethylmercury (DMHg) for reasons of economy. Moreover, DMHg is extremely stable; its use would necessitate thermal pre- cracking, or limit direct growth to 500°C.

Using elemental mercury, the growth temperature of MCT is dictated by the ease of decomposition of the Te source. The use of DETe typically limits MCT growth to 415°C or higher temperatures. Growth with alternate chemicals such as diisopropyltelluride (DIPT) has allowed [15] reduction of the growth temperature to around 370°C, with a corresponding improvement in the resulting crystal quality. The success of DIPT has lead to an increased effort on the development and use of new organo-tellurium sources [16, 17]. A few of these are listed in Table 1, together with their cracking temperatures. As seen, a temperature of 300°C appears to be quite realistic for the growth of MCT today.

A unique problem in MCT growth, arising from the fact that elemental mercury is the commonly used Hg source, is that the reactor tube ahead of the susceptor must be kept "warm" in order to prevent mercury condensation. This results in some unavoidable premature cracking of the DMCd. For this reason, it is extremely important to prevent convective flow ahead of the susceptor, in order to avoid uncontrolled depletion of the Cd source.

The use of diisopropyltelluride (DIPT) allows the growth of MCT to be carried out at about 370°C. This chemical is now available in sufficient purity so that it has replaced DETe as a tellurium source for MCT growth. This, in turn, has already resulted in further improvements in its chemical purification. Reduction of the MCT growth temperature by the use of DIPT has many advantages. First, the Hg consumption is reduced (by a factor of 2), because of the lower partial pressure needed for MCT growth. Next, the wall temperature is reduced to around 180°C, with less depletion of the Cd-source, and less problems from convective flow. Finally, defect formation due to mismatch in thermal expansion coefficient between the MCT and the substrate is reduced by lowering the operating temperature.

It goes without saying, however, that the use of DIPT will be superceded by one or more of the sources listed in Table 1. At the present time, it is difficult to predict which of these will be the chemicals of choice, or whether still newer sources will be developed in the future. It seems reasonable, however, that the direct OMVPE growth of MCT at 250°C will be achieved in the near term, without the necessity of pre-cracking or photo-excitation.

CdTe and HgCdTe Growth:

CdTe growth can be accomplished over a relatively wide range of temperatures, 350-420°C, using DMCd and DETe. The achievement of good morphology becomes increasingly difficult at higher growth temperatures (440°C). We believe that this is due to the tendency of tellurium crystallites to form on the substrate at these temperatures. An alternative possibility is the formation of a solid methylene polymer [18], which would have the same consequence.

The growth rate of CdTe as a sub-linear function of the partial pressures of the both DMCd and DETe. This can be explained by assuming a Langmuir Hinshelwood model, where the deposition of CdTe occurs by the adsorption of these two reactants followed

by a surface catalyzed reaction. We have proposed [19] the following growth mechanism for CdTe: DMCd decomposes into Cd at the surface and gets strongly chemisorbed. On the other hand, no such reaction occurs in the case of DETe. The eventual growth of CdTe occurs by the surface reaction of DETe and the Cd.

MCT layers can be grown at 415°C when DMCd and DETe are used. A 20% Cd composition typically requires a mercury partial pressure of 0.04 atm., a DMTe partial pressure of 2.5×10^{-3} atm., and a DMCd pressure of 5×10^{-5} atm. These values, and in particular the vapor pressure of Hg, are strongly system-specific, and are provided here for illustrative purposes. Additionally, a wall temperature of 230°C is used to prevent Hg condensation.

Figures 3 and 4 shows the growth rate and composition of MCT layers as a function of temperature. The behavior illustrated here can be explained by noting that the growth rate of HgTe increases rapidly as the susceptor temperature is increased, due to increased DETe decomposition. On the other hand, the growth of CdTe is relatively constant above 400°C. Hence, the increase in growth rate in Fig. 3 is largely due to an increase in the deposition of HgTe at higher temperature. This will cause a reduction in the composition x of the layer with temperature, as seen in Fig. 4.

MCT Layer Properties:

Hg, Cd, and Te all have finite, non-unity sticking coefficients at typical reactor growth temperatures and pressures. Moreover, the growth of the separate binary components (CdTe and HgTe) is kinetically controlled. As a result, the achievement of areal compositional uniformity by direct alloy growth has been difficult with OMVPE. Our recent results, however, indicate [20] that this problem can be solved by suitable attention to reactor design. We now quote data for a reactor with a non-rotating susceptor, in the expectation that improved results can be obtained by rotation. DIPT was used as the tellurium source for this work.

Table 2 shows a map of 25% transmission cutoff points (λ_{25}) for a layer of 1 cm $\times$ 1 cm area, measured from edge to edge. Note that this represents the entire wafer, without post-growth trimming of edges. The λ_{25} value over this area corresponds to a compositional uniformity of better than ± 0.002 (σ=0.0012). On a 1 cm $\times$ 2 cm area substrate, the composition x is typically within ± 0.005 (σ=0.0023) over the whole area. For a 2 cm $\times$ 2 cm substrate area, $x \simeq \pm 0.009$, ($\sigma \simeq 0.0043$). The thickness uniformity of these layers is also excellent, better than ± 0.07 μm for 12 μm thick layers. Many layers have been grown with the above composition of $x \simeq 0.2$, and the uniformity was found to be reproducible from run to run.

Figure 5 shows the infrared transmission curve from five points on a 1 cm $\times$ 1 cm area sample. The transmission curve is relatively sharp for a composition of $x \approx 0.2$. The sharp interface between the MCT and the substrate is demonstrated by the well defined interference fringes. Excellent thickness uniformity is evident from the overlapping interference fringes of the transmission curves from different areas of the substrate, which are indicated in the figure. We believe that this is the first time such compositional uniformity has been demonstrated for OMVPE growth over this large area, using conventional alloy growth techniques.

Layers of comparable uniformity have been grown [21, 22] using an interdiffused multilayer process, where alternate layers of CdTe and HgTe are grown under optimized growth conditions for each binary compound, and homogenized at the growth temperature with an annealing step. However, this involves an interdiffusion process which requires a rather high temperature, and offsets the advantage of low temperature growth. In addition, the crystallinity of interdiffused HgCdTe layers has been shown

to be poorer than that of alloy grown HgCdTe, as determined by double crystal x-ray diffraction [23].

The structural quality of MCT can be assessed by means of x-ray double crystal diffraction. In general, the rocking curve full width half maximum can be expected to fall with reduced growth temperature, as well as with improved lattice match to the substrate. Our results, for MCT layers grown at 370°C using DIPT, indicate that the FWHM for layers grown on $CdTe_{0.96}Se_{0.04}$ substrates is 47±2 arc-sec over a 1 cm × 1 cm area, which is one of the lowest values reported for MCT epitaxial layers. Comparable values for layers grown on CdTe, under identical conditions, are 151±15 arc seconds.

X-ray measurements were also made on the CdTeSe and CdTe substrate material. Here, CdTeSe substrates had FWHM values of ≈14 arc seconds and CdTe substrates typically gave values of about 32 arc seconds. Thus, in addition to CdTeSe being better lattice matched to HgCdTe, its crystal quality is superior to that of CdTe. However, X-ray measurements on successively thinned MCT layers indicates that the significant improvement in the quality of MCT layers grown on CdTeSe substrates is primarily due to its better lattice match to the substrate.

The growth of MCT by OMVPE is carried out under conditions which result in a high concentration of Hg vacancies. Thus, layers are intrinsically p-type. However, in-situ annealing for one hour at 300°C in an Hg overpressure converts them to n-type. This is conveniently done before cool down of the reactor; in fact, care must be taken to prevent accidental type-conversion at this point in time. p-type behavior of the layers can be preserved if they are capped with 0.1 to 0.5 μm of CdTe immediately after growth, and then cooled down to room temperature.

Mobility and carrier concentration measurements have been made using a clover-leaf van der Pauw structure, and a magnetic field of 2.1 kG. Figures 5 and 6 show the results for n-type layers of various compositions. In all cases, the mobility fell by only about 7% when the applied magnetic field was increased from 2.1 to 4.5 kG, confirming that the material is truly extrinsic.

The Hall coefficient R_H for these three samples is negative at low temperatures (because an excess of donors dominate extrinsic condition), and remains negative in the intrinsic range at higher temperatures (because the electron mobility is greater than the hole mobility).

Figures 7 and 8 show the mobility and Hall coefficient for two samples with x=0.19 and x=0.26. Here, the hole concentration at 77K is in the range of 5×10^{17} cm^{-3}, and is established by the Hg overpressure during growth. The Hall mobility is in the 400-700 cm^2/V-sec range. These results indicate that the residual donor concentration in these layers is below 1×10^{15} cm^{-3}, and that the electrical quality of this material is now suitable for large area photoconductive as well as photovoltaic applications.

Conclusions

This paper has reviewed the organometallic epitaxy of HgCdTe for infrared applications, using direct alloy growth. It is shown that large area, highly uniform layers can be grown using conventional OMVPE techniques. Layers, grown in a vertical reactor without substrate rotation, had a Cd composition uniformity of ±0.005 (σ=0.0023) over a 1 cm × 2 cm area substrate. By employing a substrate rotation technique, we believe that a uniformity to better than ±0.002 ($\sigma \simeq$0.001) can be achieved over this area. The layers are electrically of very high quality, with background carrier concentration of less than 1×10^{15} cm^{-3}, for n-type material with $x \simeq$0.2.

The use of GaAs substrates gives HgCdTe layers with mobility and x-ray FWHM values which are comparable to these obtained by growth on bulk CdTe. However, the

highest quality material is obtained when lattice matched substrates such as CdTeZn or CdTeSe are used. The use of CdTeSe substrates instead of CdTe gives HgCdTe layers with improved crystal quality as determined by double crystal x-ray diffraction data. The FWHM value for $Hg_{0.8}Cd_{0.2}Te$ grown on $CdTe_{0.96}Se_{0.04}$ is about 47 arc seconds, which is one of the lowest value reported for this material, and about three times smaller than that for layers grown simultaneously on CdTe substrates.

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TABLE 1: ALTERNATE TELLURIUM SOURCES

		VAPOR PRESSURE	GROWTH
1. DIMETHYLTELLURIDE DMTE, $(CH_3)_2Te$	L	51 TORR AT 25°C	≈450°C
2. DIETHYLTELLURIDE DETE, $(C_2H_5)_2Te$	L	9.2 TORR AT 25°C	≈415°C
3. DIISOPROPYLTELLURIDE DIPT, $(C_3H_7)_2Te$	L	1.5 TORR AT 20°C	≈350°C
4. DIMETHYLDITELLURIDE DMDT, $(CH_3)_2Te_2$	L	4.7 TORR AT 30°C	≈300°C
5. METHYLALLYLTELLURIDE MATE, C_4H_8Te	L	25 TORR AT 42°C	≈300°C
6. DIHYDROTELLUROPHENE DHTE, C_4H_6Te	S	0.35 TORR AT 25°C	< 300°C
7. DIALLYLTELLURIDE DATE, $(C_3H_5)_2Te$	L	<1% @ 45°C OPERATION	≈300°C

TABLE 2: MAP OF 25% TRANSMISSION CUTOFF POINTS FOR A 1.0μ x 1.0μ LAYER

9.08	9.09	9.17	9.17	9.20	9.15	9.10	9.08	
9.07	9.23	9.19	9.19	9.19	9.19	9.19	9.10	9.28
9.14	9.25	9.25	9.23	9.23	9.23	9.28	9.28	9.36
9.29	9.28	9.31	9.25	9.31	9.31	9.31	9.31	9.41
9.38	9.23	9.23	9.25	9.33	9.36	9.36	9.33	9.58
9.33	9.18	9.23	9.28	9.36	9.38	9.38	9.31	9.61
9.23	9.10	9.23	9.25	9.31	9.31	9.31	9.31	9.52
	9.13	9.23	9.23	9.31	9.36	9.31	9.38	9.44

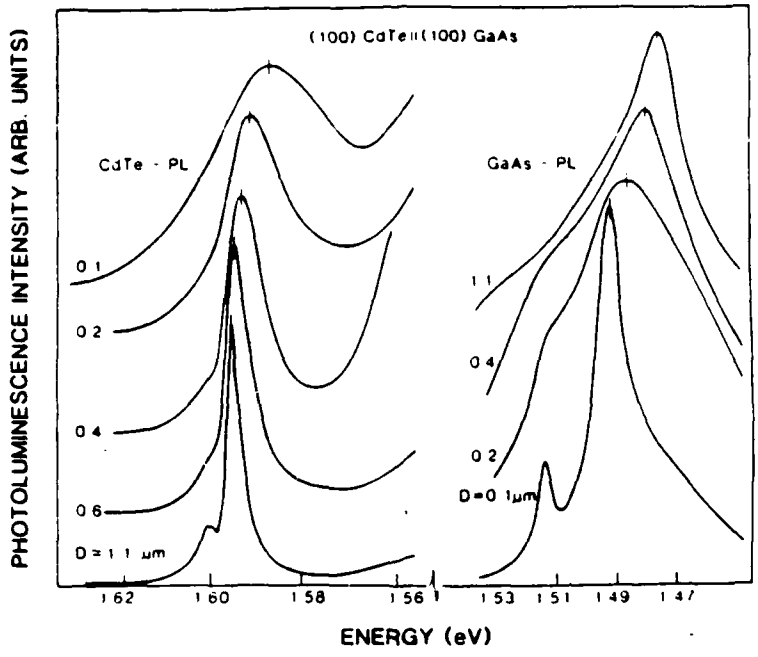


FIG. 1 PL INTENSITY OF CDTE ON GAAS, AS A FUNCTION OF CDTE LAYER THICKNESS. ALSO SHOWN IN PL DATA FOR THE GAAS SUBSTRATE.

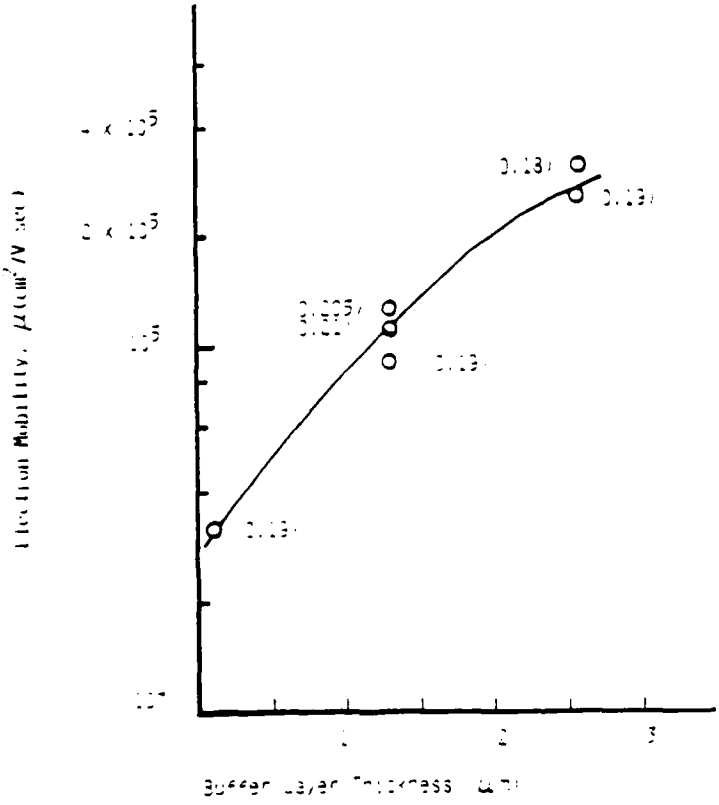
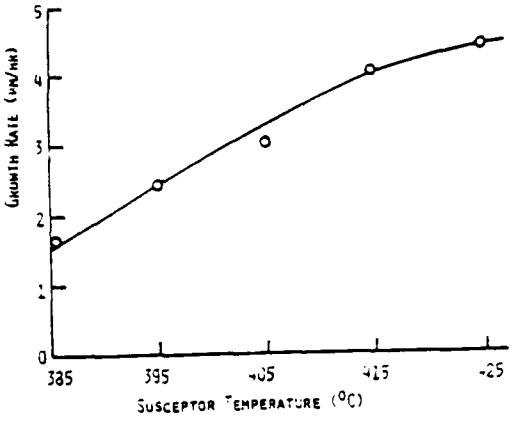


FIG. 2 MOBILITY OF MCT GROWN ON GAAS AS A FUNCTION OF CDTE BUFFER LAYER THICKNESS.



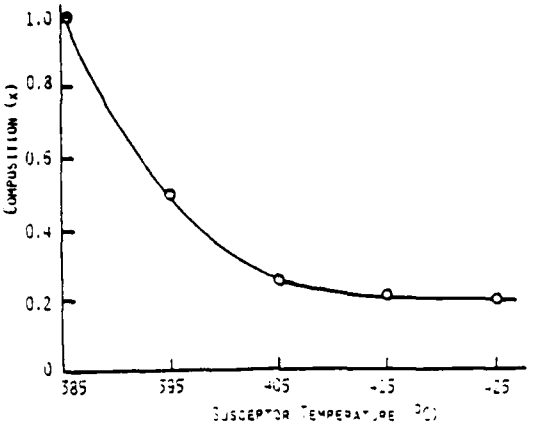


FIG. 3 GROWTH RATE OF MCT LAYERS VERSUS SUSCEPTOR TEMPERATURE. P_{HG}=0.04 ATM, P_{DMCD}=4 x 10^{-5} ATM, P_{DETE}=2.5 x 10^{-3} ATM.

FIG. 4 VARIATION IN THE COMPOSITION OF x AS A FUNCTION OF THE SUSCEPTOR TEMPERATURE, FOR THE SAME REACTOR CONDITION AS SHOWN IN FIG. 3.

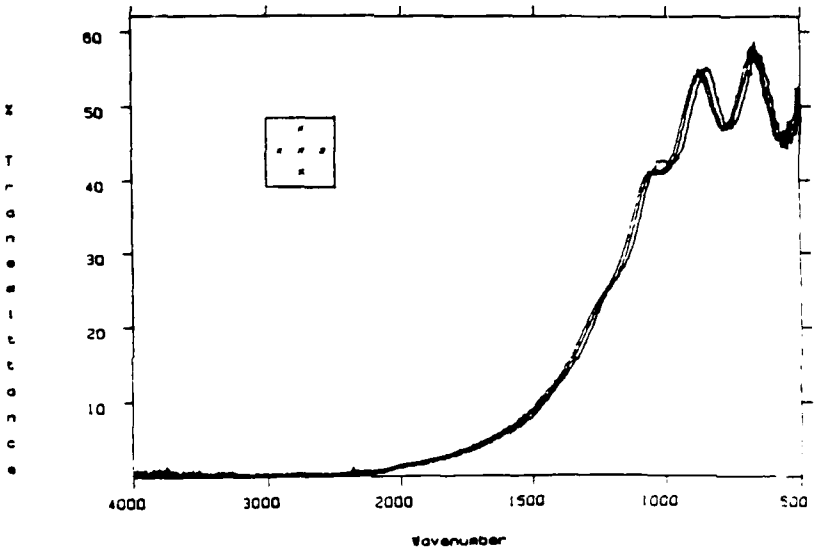


FIG. 5 TRANSMISSION SPECTRUM OF [illegible]

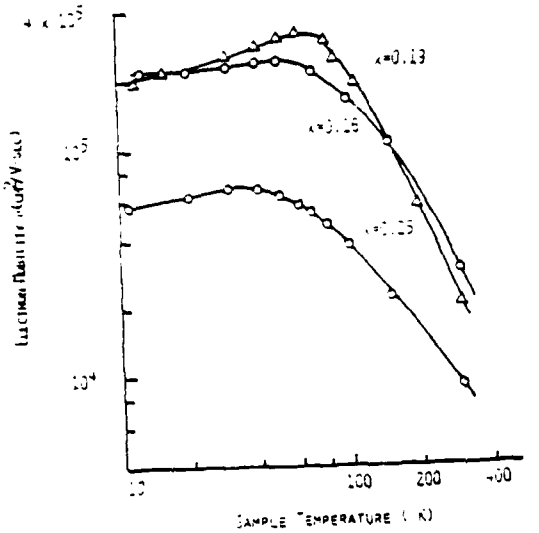


FIG. 6 HALL MOBILITY AS A FUNCTION OF TEMPERATURE.

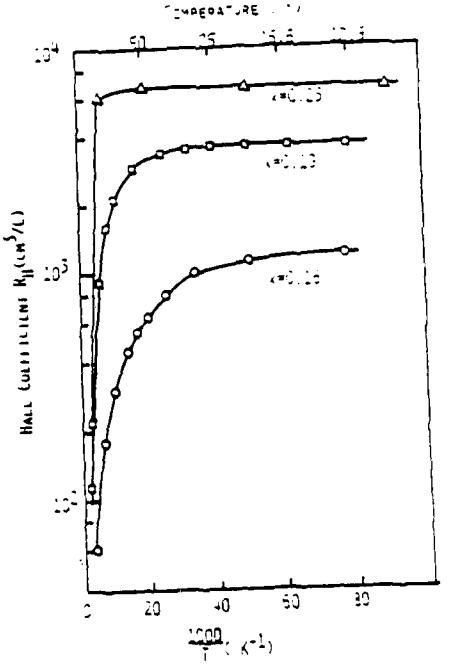


FIG. 7 HALL COEFFICIENT FOR THE SAMPLES OF FIG. 6.

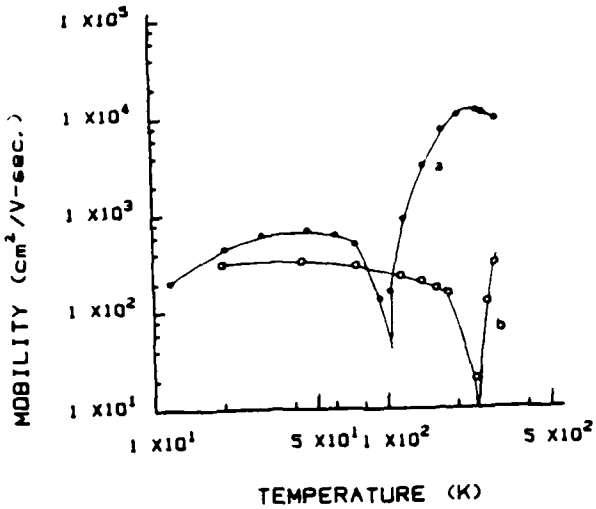


FIG. 8 HALL MOBILITY FOR TWO P-TYPE SAMPLES.

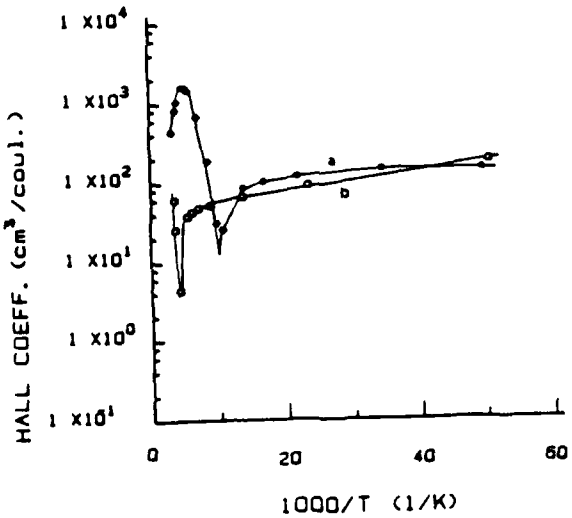


FIG. 9 HALL COEFFICIENT FOR THE SAMPLES OF FIG. 8.

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